ELECTRONIC DESIGN AUTOMATION
(ECEN 3106)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Minimum Number of Transistors in CMOS Logic Y = ABC + DE is
(a) 8 (b) 10 (c) 12 (d) 14

(ii) The threshold voltage of an ideal inverter is
(a) VDD (b) $V_{DD}/2$ (c) $V_{DD}/4$ (d) $V_{DD}/3$

(iii) Memory Design is normally done using below Design Approach
(a) FPGA (b) Gate Array
(c) Full Custom Design (d) Standard Cell Based Semi Custom Design

(iv) The Programmable Array Logic (PAL) consists of
(a) Programmable AND & OR plane
(b) Programmable AND & fixed OR plane
(c) Fixed AND & programmable OR plane
(d) Fixed AND & OR plane

(v) In λ-based design rule system, the minimum feature size is taken to be
(a) λ (b) 2λ (c) 3λ (d) λ/2

(vi) Basic tasks to perform in high level synthesis include
(a) Operation scheduling (b) Datapath and control allocation
(c) Module binding (d) All of the above

(vii) The ^ operator in verilog signifies
(a) bit-wise OR (b) bit-wise XOR
(c) logical OR (d) logical XOR

(viii) Purpose of Floorplanning is
(a) Optimizing Chip Area (b) Optimizing Total Wire Length
(c) Ensuring Routability (d) All of Above

(ix) Maze Routing is
(a) 2 Terminal Routing (b) 3 Terminal Routing
(c) 4 Terminal Routing (d) 5 Terminal Routing.

(x) Objectives of routing include minimization of
(a) area of the chip (b) total wire length in the chip
(c) net delay on critical paths (d) all of the above

Fill in the blanks with the correct word

(xi) The Euler path traverses each edge (branch) of the graph exactly _____.

(xii) Noise immunity _____ with noise margin.

(xiii) Global routing generates a _____ route for each net.

(xiv) In Micron-based design rule system, layout constraints are stated in terms of absolute dimensions in _____.

(xv) D-latch is a _____(level sensitive/edge triggered) circuit.

Group - B

2. (a) Implement 2 input XOR Gate using Transmission Gate Logic. *[(CO2)(Analyse/IOCQ)]*
(b) Implement Positive D-Latch (Level-1) using Transmission Gate Based Circuit. *[(CO3)(Analyse /IOCQ)]*
(c) Implement Negative Edge Triggered Flip-Flop using Positive D-Latch and any Digital CMOS Combinational Logic Gate. *[(CO3)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

3. (a) Design a sequential circuit which obeys the following truth table :

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

[(CO3)(Apply/IOCQ)]

(b) Analyze positive and negative latches using transmission gate multiplexers. *[(CO3)(Analyze/IOCQ)]*
(c) Draw the stick diagram layout of the function $f = ((A + B + C + D). E)'$ *[(CO3)(Create/HOCQ)]*

4 + 3 + 5 = 12

Group - C

4. (a) Explain the differences between Full Custom Design and Standard Cell based Semi Custom Design. *[(CO1)(Analyse/IOCQ)]*
(b) Implement Y = ABC + AC + BC using PLA. *[(CO1)(Evaluate/HOCQ)]*

6 + 6 = 12

5. (a) Construct an Euler Path for the function, Y=(A(D+E)+(BC))'. *[(CO1)(Create/HOCQ)]*
(b) Build the stick diagram for the above function in (a). *[(CO1)(Create/HOCQ)]*

6 + 6 = 12

Group - D

6. (a) Illustrate Ordered (OBDD) and Isomorphic Binary Decision Diagram. *[(CO5)(Understand/LOCQ)]*
(b) Construct a BDD for the function f = abc + ab'c + a'bc' + a'b'c' with the variable ordering c ≤ b ≤ a. *[(CO5)(Apply/IOCQ)]*
(c) Draw a BDD for the OR function. *[(CO5)(Apply/IOCQ)]*

4 + 5 + 3 = 12

7. (a) Construct the flow diagram to show the phases or tasks involved in High Level Synthesis. *[(CO4)(Apply/IOCQ)]*
(b) (i) Determine the type of compiler-based transformation that is required in a typical program that might consist of the following statements.
D=A+B+C;
F=A+B+E;
(ii) How is the transformation carried out?
(iii) What advantage do we get by making such a transformation? *[(CO4)(Analyze/IOCQ)]*
(c) List the four types of Scheduling problems. *[(CO4)(Remember/LOCQ)]*

5 + 3 + 4 = 12

Group - E

8. (a) Briefly discuss the factors to be considered for floor planning. *[(CO6)(Understand/LOCQ)]*
(b) Consider Fig. 1 with the initial partition *U = {a, b, d, e}* and *V = {c, f, g, h}.* Apply K-L partitioning algorithm and compute all possible gain pairs for (U, V) node swapping. Evaluate the node swapping that provides maximum gain at the end of this iteration? *[(CO6)(Evaluate/HOCQ)]*

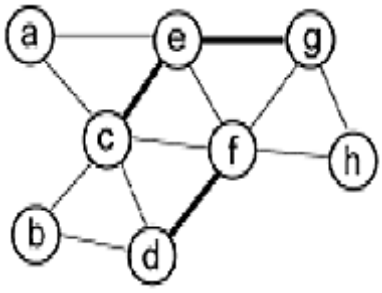

Fig. 1

6 + 6 = 12

9. (a) Mention the objectives of routing. *[(CO6)(Remember/LOCQ)]*
(b) Distinguish between global and detailed routing. *[(CO6)(Understand/LOCQ)]*
(c) Why is multilevel routing necessary? Differentiate the reserved and the unreserved layer routing models. *[(CO6)(Analyze/IOCQ)]*

2 + 4 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	20.83	44.79	34.38