LOW POWER VLSI DESIGN
(VLSI 5232)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) The most significant component of static power dissipation in CMOS circuits is
(a) diode leakage current (b) gate leakage
(c) subthreshold leakage (d) glitch power.

(ii) Short circuit power dissipation takes place due to
(a) slow changing inputs (b) fast changing inputs
(c) constant inputs (d) no input.

(iii) Maximum leakage power contribution comes from
(a) channel leakage (b) gate leakage of ON Transistor
(c) junction leakage (d) gate leakage of OFF Transistor.

(iv) Parallel-pipelined realization of a circuit might involve a reduction of
(a) only the supply voltage
(b) frequency of operation
(c) both supply voltage and frequency of operation
(d) area.

(v) As channel length is reduced,
(a) delay increases (b) power decreases
(c) delay decreases but power increases (d) delay and power increase.

(vi) DVFS stands for
(a) Dramatic Voltage and Frequency Scaling
(b) Derived Voltage and Frequency Scaling
(c) Dynamic Voltage and Frequency Scaling
(d) Device Voltage and Frequency Scaling.

(vii) High V_{dd} gates are usually associated with a
(a) high delay (b) low delay (c) zero delay (d) infinite delay.

(viii) Dynamic power dissipation includes
(a) switching power dissipation
(b) diode leakage current
(c) glitching power, switching power and short circuit power
(d) subthreshold leakage.

(ix) Both power and delay reduction for a digital gate is possible if
(a) CL decreases (b) V_{DD} decreases
(c) activity factor decreases (d) never possible.

(x) Glitch power can be reduced by implementing
(a) cascaded form (b) balanced form
(c) inserting buffers (d) both (b) and (c).

Fill in the blanks with the correct word

(xi) Pull up network consists of _____transistors.

(xii) Switching power dissipation is a type of _____ (static/dynamic) power dissipation.

(xiii) NMOS transistors make up the _____ network in a CMOS circuit.

(xiv) The subthreshold current is dependent on the substrate bias. ____ (True/False).

(xv) The switching power dissipation is _____ (dependent/independent) of the device parameters.

Group - B

2. (a) What do you mean by short circuit power dissipation in CMOS circuits? *[(CO4)(Remember/LOCQ)]*
(b) Outline the cause of origin of short circuit power dissipation in the CMOS circuits. *[(CO2)(Understand/LOCQ)]*
(c) Develop an expression for the short circuit power and analyze the possible means of reducing it. *[(CO1)(Analyze/IOCQ)]*

1 + 1 + 10 = 12

3. (a) Explain how switching power dissipation takes place in a typical CMOS circuit. *[(CO1)(Remember/LOCQ)]*
(b) What is switching activity in CMOS gates? *[(CO2)(Understand/LOCQ)]*
(c) Calculate the probability of transition of a NOR gate considering equiprobable inputs. *[(CO2)(Evaluate/HOCQ)]*

5 + 2 + 5= 12

Group - C

4. (a) What is static power dissipation? *[(CO3)(Analyse/HOCQ)]*
(b) Classify all the different components of the leakage currents that lead to static power dissipation in CMOS circuits. Illustrate with a suitable diagram. *[(CO3)(Analyze/IOCQ)]*

(c) Mention any four mechanisms in which threshold voltage of a MOSFET can affect the subthreshold leakage. *[(CO3)(Remember/LOCQ)]*

2 + 8 + 2 = 12

5. (a) Differentiate between Fowler-Nordheim tunnelling and direct tunnelling with suitable diagrams. *[CO3/Understand/LOCQ]*

(b) How does gate leakage occur due to hot electrons? *[CO3/Understand/LOCQ]*

8 + 4 = 12

Group - D

6. (a) Show how parameters like power dissipation and the power dissipation density are affected in the two types of scaling techniques. Hence, comment on the suitability of the scaling techniques in low power VLSI applications. *[(CO5)(Apply/IOCQ)]*

(b) Mention the different voltage scaling approaches used for the reduction in power dissipation in VLSI circuits. *[(CO5)(Remember/IOCQ)]*

8 + 4 = 12

7. (a) What is glitch power? Explain with a suitable example. *[(CO3)(Understand/LOCQ)]*

(b) How can glitch power dissipation be reduced? *[(CO2)(Apply/IOCQ)]*

(c) Name the various components of the load capacitance (C_L) in digital VLSI circuits. *[(CO1)(Remember/LOCQ)]*

6 + 2 + 4 = 12

Group - E

8. (a) Why is it preferable to use constant-field scaling over constant-voltage scaling in the context of low power? *[(CO6)(Apply/IOCQ)]*

(b) Justify the use of pipelining in low power VLSI circuits. *[(CO6)(Analyze/IOCQ)]*

6 + 6 = 12

9. (a) What is parallel processing? *[(CO4)(Remember/LOCQ)]*

(b) What are the advantages of using a parallel architecture in VLSI design? *[(CO3)(Understand/IOCQ)]*

(c) Show how parallelism can be used to achieve low power instead of high performance in realizing a 16 bit adder circuit. *[(CO4)(Apply/IOCQ)]*

1 + 1 + 10= 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	35.42	57.29	7.29

Course Outcome (CO):

After the completion of the course students will be able to
1. Students will learn source of CMOS Dynamic Power Dissipation
2. Students will learn CMOS Dynamic Power Reduction Techniques

3. Students will learn source of CMOS Standby (leakage) Power Dissipation & Reduction Techniques
4. Students will learn Short Circuit Power Reduction Techniques
5. Students will learn Embedded Memory Power Reduction Techniques
6. Students will learn System and Architecture level Power Reduction Techniques

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*