DIGITAL SYSTEMS DESIGN
(ECEN 2202)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) The code where all successive numbers differ from their preceding number by single bit is
(a) Alphanumeric Code (b) BCD
(c) Excess 3 (d) Gray.

(ii) The simplified form of the Boolean expression (X+Y+XY)(X+Z) is
(a) X+Y+Z (b) XY+YZ
(c) X+YZ (d) XZ+Y.

(iii) In which of the following adder circuits is the carry ripple delay eliminated?
(a) Half-adder (b) Full-adder
(c) Parallel-adder (d) Carry-look ahead adder.

(iv) How many possible outputs would a decoder have with a 6-bit binary input?
(a) 32 (b) 64 (c) 128 (d) 16.

(v) What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
(a) 0 to 2^n (b) 0 to $2^n + 1$
(c) 0 to $2^n - 1$ (d) 0 to $2^{n+1/2}$.

(vi) A universal register
(a) accepts serial input (b) accepts parallel input
(c) give serial and parallel outputs (d) is capable of all of the above

(vii) The number of flip-flops required for a mod-16 ring counter is
(a) 4 (b) 8 (c) 15 (d) 16

(viii) In general, a sequential logic circuit consists of
(a) only flip-flops
(b) only gates
(c) flip-flops and combinational logic circuits
(d) only combinational logic circuits.

(ix) Which family has the better noise margin?
(a) ECL (b) DTL (c) MOS (d) TTL.

(x) Which logic family uses transistor in a totem-pole configurations?
(a) TTL (b) CMOS (c) ECL (d) DTL

Fill in the blanks with the correct word

(xi) In a multiplexer, the selection of a particular input line is controlled by _____.

(xii) 2's complement of binary number 0101 is _____.

(xiii) The basic storage element in a digital system is _____.

(xiv) Minimum number of 2-input NAND gates required to implement the function F = (x + y) (Z + W) is _____.

(xv) Maxterm designation for A + B + C is _____.

Group - B

2. (a) Find the minimal sum of the products for the Boolean expression *f(A,B,C,D)=∑m(1,2,3,7,8,9,10,11,14,15)* using Quine-McCluskey method. *[CO1/Apply/IOCQ]*

(b) Simplify the expression *Y=∑m(3,4,5,7,9,13,14,15) using the K-map and realize the function using NAND gates only.* *[CO1/Evaluate/HOCQ]*

6 + 6 = 12

3. (a) Express the function $Y = (\bar{Y} + WZ)$ into canonical SOP and canonical POS form. *[CO1/Apply/LOCQ]*

(b) Design a BCD to Excess-3 code conversion circuit using basic gates. *[CO1/Evaluate/LOCQ]*

6 + 6 = 12

Group - C

4. (a) What are the basic differences between EPROM and EEROM? *[(CO6)(Remember, Analyze /LOCQ)]*

(b) With the help of a logic diagram and a truth table, explain an Octal to Binary encoder. *[(CO2)(Apply/IOCQ)]*

(c) Implement the following function using PROM (i) *A= f(A,B,C)=∑m(5,6,7), (ii) B= f(A,B,C)=∑m(3,5,6,7).* *[(CO6)(Apply/LOCQ)]*

2 + 4 + 6 = 12

5. (a) Implement the following function using 8:1 MUX:
F(A, B, C, D)=∑m(1, 3, 4, 11, 12, 13, 14, 15). *[(CO2) (Evaluate /HOCQ)]*

(b) Realize a Full Adder Circuit using 3 to 8 Decoder. *[(CO2) (Analyze /IOCQ)]*

6 + 6 = 12

Group - D

6. (a) Draw the gate level circuit diagram of a positive edge-triggered JK flip-flop and explain its operation with the help of a truth table. How the race around condition eliminated? *[(CO3)(Remember/LOCQ)]*

   (b) What is a shift register? Distinguish between a shift register and a counter. *[(CO3)(Remember/LOCQ)]*

   (c) Realize D flip-flop using J-K flip-flop. *[(CO3)(Evaluate/IOCQ)]*

(3 + 2) + 3 + 4 = 12

7. (a) A clocked sequential circuit has four states A, B, C and D as show in the state diagram of Fig.1. Assume state assignments as A=00, B=01, C=10 and D=11. Prepare the state table and draw circuit using D flip-flops. *[(CO3)(Evaluate/HOCQ)]*

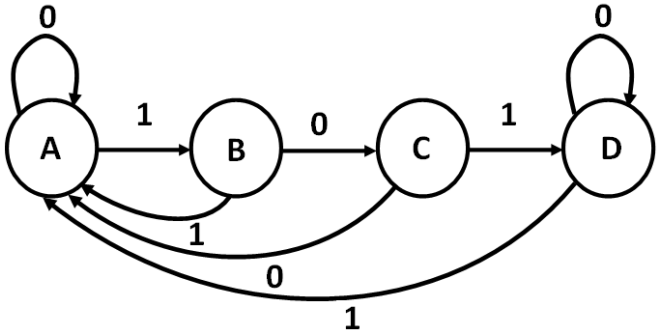

Fig. 1: State diagram of a clocked sequential circuit

   (b) Design a synchronous MOD 3 UP/DOWN Counter using D flip-flops. *[(CO3)(Evaluate/LOCQ)]*

6 + 6 = 12

Group - E

8. (a) Explain the operation of a Flash type ADC with proper circuit diagram. *[(CO4)(Remember/IOCQ)]*

   (b) Explain the operation of a 4-bit R-2R ladder type DAC with proper circuit diagram. *[(CO4)(Remember/IOCQ)]*

6 + 6 = 12

9. (a) Draw a NOR Gate using RTL logic circuit. *[(CO5)(Remember/LOCQ)]*

   (b) Design a CMOS NOT gate and explain its operation. *[(CO5)(Remember/LOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	47.9	33.3	18.8

Course Outcome (CO):

After the completion of the course students will be able to

1. Make use of the concept of Boolean algebra to minimize logic expressions by the algebraic method, K-map method, and Tabular method.
2. Construct different Combinational circuits like Adder, Subtractor, Multiplexer, De-Multiplexer, Decoder, Encoder, etc.
3. Design various types of Registers and Counters Circuits using Flip-Flops (Synchronous, Asynchronous, Irregular, Cascaded, Ring, Johnson).
4. Outline the concept of different types of A/D and D/A conversion techniques.
5. Realize basic gates using RTL, DTL, TTL, ECL, and CMOS logic families.
6. Relate the concept of Flip flops to analyze different memory systems including RAM, ROM, EPROM, EEROM, etc.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question