ANALOG & DIGITAL ELECTRONICS
(ELEC 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The slew rate of an operational amplifier should be
(a) zero (b) unity
(c) as small as possible (d) as large as possible

(ii) If a square wave is applied at the input of an integrator circuit using operational amplifier then the output waveform is
(a) sinusoidal (b) parabolic
(c) square (d) triangular

(iii) The fundamental frequency of a crystal oscillator is
(a) directly proportional to the temperature of the crystal
(b) directly proportional to the thickness of the crystal
(c) inversely proportional to the thickness of the crystal
(d) inversely proportional to the thickness of the crystal

(iv) The input terminals of an ideal operational amplifier are at the same potential because
(a) the two input terminals are directly shorted to ground
(b) the differential input resistance is infinite
(c) the differential input resistance is zero
(d) the open loop gain is infinite

(v) To avoid false triggering the RESET pin of 555 timer is connected to
(a) Ground (b) Trigger
(c) Discharge (d) $+V_{CC}$

(vi) Which of the following is a weighted code?
(a) 2421 (b) Excess-3
(c) Gray (d) All of the above

(vii) Convert the following binary number to gray code: $(10110)_2$
(a) 11001 (b) 11101
(c) 10011 (d) 01101

(viii) The minimum number of flip flops required to design a MOD-10 counter is
(a) 03 (b) 10
(c) 04 (d) 05

(ix) A feature that distinguishes the J-K flip-flop from the S-R flip flop is the
(a) toggle condition (b) preset input
(c) type of clock (d) clear input

(x) Why is a Demultiplexer called a data distributor?
(a) The input will be distributed to one of the outputs
(b) One of the inputs will be selected for the output
(c) The output will be distributed to one of the inputs
(d) Single input gives single output

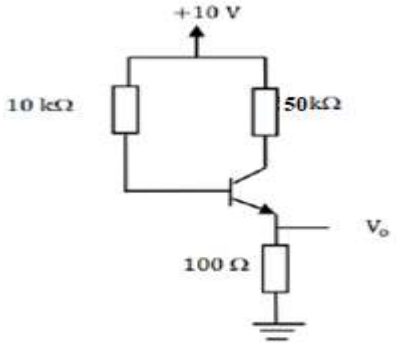
Group – B

2. (a) Design a subtractor circuit using only one operational amplifier to obtain an output voltage $V_o = 3V_2 - 4V_1$ where V_1 and V_2 are the input voltages.

(b) Realise the linear differential equation using minimum number of operational amplifier:

$$\frac{d^2y}{dt^2} + 4\frac{dy}{dt} + 2y = 5$$

(c) The transistor circuit shown below uses a silicon transistor with V_{BE} = 0.7V, $I_C \approx I_E$ and β = 100. Determine the values of I_C and V_o.



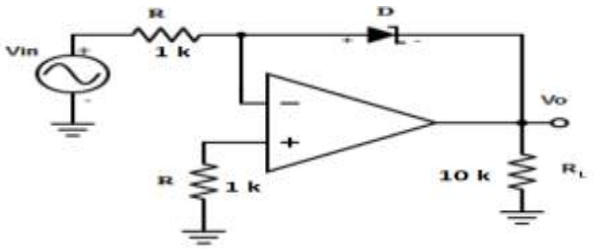
4 + 4 + 4 = 12

3. (a) Explain the principle of operation of a peak detector circuit using operational amplifier with the help of a neat diagram.

(b) Draw the output voltage waveform of a non-inverting comparator circuit where the input voltage is 10Vp-p sine wave and the reference voltage is 1V. Also draw the transfer characteristics.

(c) Consider the circuit shown in the figure below. If V_Z = 6V and voltage drop across forward biased Zener diode = 0.7V, determine the output voltage

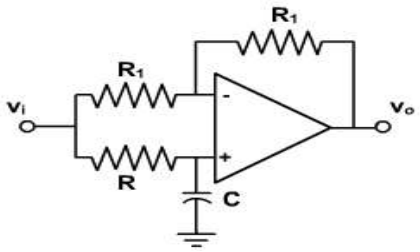
waveform. Assume the input voltage is a sine wave of 15Vp-p and saturation voltages are ±15V.



4 + 4 + 4 = 12

Group – C

4. (a) Show that, the op-amp phase shifter shown below has gain $\frac{V_o}{V_i} = \frac{1-j\omega RC}{1+j\omega RC}$.



(b) The following specifications are given for voltage regulator LM566: V_{CC} = 12V and control voltage V_C = 10V. Design the circuit to obtain an output waveform with nominal frequency 25kHz. Also determine the modulation in the output frequency if V_C is varied between 7.5V and 11.5V.

(c) Design an astable multivibrator using 555 timer with oscillation frequency f_o = 1.5kHz and duty cycle = 60%.

4 + 4 + 4 = 12

5. (a) Draw a neat diagram of Wien bridge oscillator using operational amplifier. Derive the expression of oscillation frequency. Also determine the gain at the oscillation frequency. Hence design a Wien bridge oscillator with oscillation frequency f_o = 1kHz.

(b) Discuss the principle of operation of an astable multivibrator using IC555 with the help of a neat circuit diagram. Sketch the output and capacitor voltage waveforms. Derive the expressions of time period of the output waveform and the duty cycle.

6 + 6 = 12

Group – D

6. (a) Construct the following: (i) Ex-OR gate using NAND gate, (ii) Ex-NOR gate using NOR gate.

(b) Apply the knowledge of K map to simplify the following Boolean function and implement it using suitable logic gates: $F(A,B,C,D) = \sum_m(1,5,6,12,13,14) + \sum d(2,4)$.

(c) Design a full Subtractor using NAND gate only.

4 + 4 + 4 = 12

7. (a) Form a multiplexer tree to give a 16×1 MUX from two 8×1 MUX.

   (b) Explain in detail how will you implement the following Boolean function using MUX: $F(A,B,C,D) = \sum_m (2,4,6,7,9,10,11,12,15)$.

   (c) Expand the expression to a standard SOP form: Y=AB+ACD.

4 + 4 + 4 = 12

Group – E

8. (a) Design a JK flip flop using a D flip flop.

   (b) Explain Race around condition related to JK flip flop. Draw the Master/Slave JK flip flop using all NAND gates and explain its working.

6 + 6 = 12

9. (a) Design a 3 bit shift register and explain its working for left shift mode.

   (b) Design a 4 bit asynchronous up counter and explain its working.

   (c) Design a 4 bit shift register using D flip flop and explain its operation for right shift mode.

4 + 4 + 4 = 12

Department & Section	Submission Link
EE regular students	https://classroom.google.com/c/MTQxOTk3Njk3MjYz/a/MjcxNjQ0MTY2OTc5/details
EE backlog students	https://classroom.google.com/c/MjQ4OTQ5OTkyNjMy/a/Mjc0MDYwOTI0NTg3/details