B.TECH/EE/3RD SEM/ELEC 2101 (BACKLOG)/2020

ANALOG & DIGITAL ELECTRONIC CIRCUITS
(ELEC 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) CMRR is the abbreviated form of
(a) Common mode rejection ratio (b) Common mode resistance ratio
(c) Constant mode rejection ratio (d) Constant mode resistance ratio.

(ii) If the input waveform of a differentiator circuit is a step signal then the output waveform is
(a) Square (b) Impulse
(c) Triangular (d) Sine.

(iii) Output waveform of Schmitt trigger circuit is
(a) Sine (b) Impulse
(c) Square (d) Parabola.

(iv) Hartley oscillator using operational amplifier consists of
(a) 1 inductor and 1 capacitor (b) 1 inductor and 2 capacitors
(c) 2 inductors and 1 capacitor (d) 2 inductors and 2 capacitors.

(v) According to Barkhausen criteria the loop gain should be equal to
(a) 1 (b) 2
(c) 3 (d) 29.

(vi) Which of the following is a weighted code?
(a) 2421 (b) Excess-3
(c) Gray (d) All of the above.

(vii) The minimum number of NAND gates required to implement an Ex-OR gate is
(a) 02 (b) 04
(c) 03 (d) 05.

(viii) The Boolean expression $\overline{A}B\overline{C}\overline{D}$ is a
(a) a sum term (b) a product term
(c) a literal term (d) always 1.

(ix) A digital multiplexer is a combinational circuit that selects
(a) One digital information from several sources and transmits the selected one via a single output
(b) Many digital information and convert them into one
(c) Many decimal inputs and transmits the selected information
(d) Many decimal outputs and accepts the selected information.

(x) If Q = 0, the output is said to be
(a) Set (b) Reset
(c) Previous state (d) Current state.

Group – B

2. (a) Draw a neat diagram of a subtractor circuit using operational amplifier. Also derive the expression of output voltage.

(b) Realise the linear differential equation using minimum number of operational amplifier:

$$\frac{d^2y}{dt^2} + 4\frac{dy}{dt} + 2y = 5$$

6 + 6 = 12

3. (a) The input resistance of an operational amplifier increases with negative feedback. Justify the statement.

(b) Show that the differential gain of a dual input balanced output differential amplifier using BJT is given by

$$\frac{v_o}{v_{id}} = g_m * R_c$$

where v_o is the output voltage, v_{id} is the differential input voltage, g_m is the transconductance and R_c is the collector resistance.

4 + 8 = 12

Group – C

4. (a) Draw a neat circuit diagram of a monostable multivibrator using 555 timer. Explain its principle of operation. Derive the expression of the time period for the metastable state.

(b) Explain line and load regulation.

10 + 2 = 12

5. (a) Draw a neat diagram of a zero crossing detector circuit. Explain its principle of operation. Draw the output voltage waveform and transfer characteristics for 10V p-p sine wave input.

   (b) Discuss the principle of operation of Colpitts oscillator with the help of a neat circuit diagram. Derive the expression of oscillation frequency.

7 + 5 = 12

Group – D

6. (a) Design a full adder using NAND gate only.

   (b) Apply the knowledge of K map to simplify the following Boolean function and implement it using suitable logic gates:
   $F(A,B,C,D) = \sum_m (0,1,2,8,10,11,14,15) + \sum_d (3,13)$

6 + 6 = 12

7. (a) Design the following Boolean function using suitable MUX
   $F= \sum_m(1,5,6,12,13,14)$

   (b) Explain the working of a 3:8 decoder.

6 + 6 = 12

Group – E

8. (a) State the difference between asynchronous and synchronous counter.

   (b) Explain how JK flip flop can be used as a frequency divider circuit.

   (c) Design a SR flip flop using JK flip flop.

2 + 4 + 6 = 12

9. (a) Design a 3 bit synchronous up counter and explain its working principle.

   (b) Design a 3 bit SISO shift register and explain its working principle.

6 + 6 = 12

Department & Section	Submission Link
EE	https://classroom.google.com/c/MjQ4OTQ5OTkyNjMy/a/MjcxNjQ3Mzk5OTI4/details