COMPUTER ORGANIZATION AND ARCHITECTURE
(CSBS 2202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The speedup of a k-stage pipelined processor to complete n tasks, compared to a non-pipelined processor is
(a) n / (k+n -1) (b) n / (k*n -1)
(c) n*k / (k+n-1) (d) n*k / (k*n -1).

(ii) In case of, zero-address instruction method the operands are stored in _____
(a) registers (b) accumulators
(c) pushdown stack (d) cache.

(iii) Instruction cycle is
(a) fetch-decode-execution (b) fetch-execution-decode
(c) decode-fetch-execution (d) none of these.

(iv) Booth's algorithm is used for
(a) multiplication of numbers in sign- magnitude form
(b) division of numbers in sign- magnitude form
(c) multiplication of numbers in 2's complement form
(d) division of numbers in 2's complement form.

(v) Superscalar pipeline have CPI of
(a) 1 (b) greater than 1
(c) less than 1 (d) greater than 2.

(vi) The addressing mode which makes use of in-direction pointers is _____
(a) indirect addressing mode (b) index addressing mode
(c) relative addressing mode (d) none of the above.

(vii) Address for the next executable instruction is stored in the
(a) stack pointer (b) program counter
(c) instruction register (d) none of these.

(viii) The CISC stands for _____.
(a) Computer Instruction Set Compliment
(b) Complete Instruction Set Compliment
(c) Computer Indexed Set Components
(d) Complex Instruction Set Computer

(ix) A stack organized computer uses
(a) indirect addressing (b) index addressing
(c) zero addressing (d) two addressing.

(x) How many address lines are needed to address each memory location in 2046 × 8 memory chip?
(a) 8 (b) 10 (c) 11 (d) 12.

Group- B

2. (a) Perform each step of the restoring division algorithm while dividing 8 by 3. [(CO2)(Apply/IOCQ)]
(b) Evaluate the arithmetic statement X = (A + B) - (C + D) using (i) zero address instructions and (ii) two address instructions. [(CO3)(Analyse/IOCQ)]
6 + (3 + 3) = 12

3. (a) Discuss the principle of carry look-ahead adder. What are the advantages and disadvantages of CLA over RCA? [(CO2)(Understand/LOCQ)]
(b) Design a 4 bit CLA. [(CO2)(Apply/IOCQ)]
(5 + 2) + 5 = 12

Group - C

4. (a) According to the information, determine the number of bits of the subfields in the address for direct mapping, associative mapping and set-associative cache schemes.
Main memory size: 256 MB
Cache memory size: 1 MB
Address space of the processor: 256 MB
Block size: 128 bytes
There are 8 blocks in a set. [(CO4)(Apply/IOCQ)]
(b) A three level memory system having cache access time of 15 ns and disk access time of 80 ns. The cache main memory hit ratio of 0.96 and main memory hit ratio of 0.9. What should be the main memory access time to achieve effective access time of 25 ns? [(CO4)(Apply/IOCQ)]
6 + 6 = 12

5. (a) A block set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16384 blocks and each block contains 256 eight bit words.
(i) How many bits are required for addressing the main memory?

(ii) How many bits are needed to represent the tag, set and word offset fields? [(CO4)(Apply/IOCQ)]

(b) "Size of a page influences the performance of a virtual memory system" – justify [(CO4)(Evaluate/HOCQ)]

(c) How does the size of cache block affect the system's performance? [(CO4)(Evaluate/HOCQ)]

(2 + 4) + 3 + 3 = 12

Group - D

6. Consider the Reservation Table given below:

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

(i) Determine the set of Forbidden Latencies and Permissible Latencies, and the Initial Collision Vector.

(ii) Draw the state diagram for scheduling this pipeline

(iii) List all simple cycles. Especially point out the Greedy Cycles (GC).

(iv) What is the Minimum Average Latency (MAL) of the pipeline? Specify lower and upper bounds of MAL? [(CO5)(Apply/IOCQ)]

(3 × 4) = 12

7. (a) What is instruction level parallelism (ILP)? Explain any two techniques that can be used for improving ILP with suitable examples as necessary. [(CO5)(Remember/LOCQ)]

(b) Discuss the different types of vector instruction and their formats. [(CO5)(Remember/LOCQ)]

6 + 6 = 12

Group - E

8. (a) Draw the data flow graph to represent the following sequence of computations:
(i) A= P + Q
(ii) B=A / Q
(iii) C=P*A
(iv) D=C-B
(v) E=C*A
(vi) F=D/E. [(CO6)(Apply/IOCQ)]

(b) Write down the advantages and disadvantages of Centralized shared memory architecture and distributed shared-memory architecture. [(CO6)(Understand/LOCQ)]

6 + 6 = 12

9. (a) Compare RISC and CISC. [(CO6)(Remember/LOCQ)]
   (b) Differentiate between Data flow architecture and Control flow architecture [(CO6)(Understand/HOCQ)]
   (c) Differentiate between Super-pipelining and Superscalar pipeline architecture. [(CO6)(Understand /LOCQ)]

6 + 3 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	35.42	55.21	9.37

Course Outcome (CO):

After the completion of the course students will be able to

1. Describe and explain the difference between computer organization and computer architecture.
2. Design the ALU for different arithmetical and logical problems and apply the knowledge of different multiplication and division algorithm.
3. Formulate design methodology for using various types of instructions.
4. Differentiate between different Memory hierarchy(Primary, Secondary, Cache). Able to solve different kind of numerical based on memory technologies and page replacement techniques.
5. Differentiate between types of pipeline, hazards and selecting remedial techniques to handle the hazards. able to distinguish between parallel architectures. Compare performance parameters of pipelines and deduce derivations to demonstrate change in performance parameters when branching is introduced. Able to solve numerical based on pipeline concepts.
6. Comparing techniques of ILP, types of CU, types of shared memory architectures. Distinguish between different multiprocessor architectures, Data Flow architecture, RISC and CISC architecture.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question