B.TECH/IT/3RD SEM/ECEN 2002/2021

DIGITAL SYSTEMS DESIGN
(ECEN 2002)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) In a 4:2 Priority Encoder, the signals at the 4 Input Lines are $I_3 = 0$, $I_2 = 1$, $I_1 = 1$, $I_0 = 0$ and at the Enable Line is E = 1, then the signals at the 2 Output Lines Y_1 and Y_0 will be ..... and ..... respectively
(a) 0, 0 (b) 0, 1 (c) 1, 0 (d) 1, 1

(ii) If $(2.3)_4 + (1.2)_4 = (y)_4$ then what is the value of y?
(a) 10.5 (b) 9.8 (c) 9.9 (d) 10.1

(iii) The Binary Number equivalent to the Gray Number 10001 is
(a) 01111 (b) 11101 (c) 11011 (d) 11110

(iv) The number of full adders and half adder required to construct an m-bit parallel adder are
(a) m/2,2 (b) m-2,2 (c) m-1,1 (d) m,0

(v) The Disabling and Enabling Logic values for OR and NOR Gates are ..... and ..... respectively
(a) 0, 1 (b) 1, 0
(c) All of the above (d) None of the Above

(vi) Which logic gate is basic comparator?
(a) NOR gate (b) NAND gate
(c) X-NOR gate (d) X-OR gate

(vii) In a CMOS NOR Gate, the 2 pMOS transistors in the Pull-Up and the 2 nMOS Transistors in the Pull Down are in .... and ..... respectively
(a) Parallel, Series (b) Series, Parallel
(c) Series, Series (d) Parallel, Parallel

(viii) How many stages a 4-bit Johnson ring counter can have?
(a) 8 (b) 4 (c) 12 (d) 16

(ix) A decoder can be converted to a demultipexer by .....
(a) doubling the number of input and output terminals
(b) adding an Enable/Signal Line to the Input
(c) All of the above
(d) None of the above

(x) The logic family that gives fastest switching is
(a) TTL (b) CMOS (c) ECL (d) RTL

Group – B

2. (a) What is the value of X for the equation given below ?
$(135)_X + (144)_X = (323)_X$. [(CO1) (Remember/LOCQ)]
(b) Implement :- (i) XOR Gate by NAND Gate
(ii) XNOR Gate by NOR Gate
(iii) NOR Gate by NAND Gate. [(CO1) (Understand/LOCQ)]
(c) Simplify the following expression :- A + B + A'.B + A.B' + A'.B' + A.B.
[(CO1) (Analyze/IOCQ)]

2 + 6 + 4 = 12

3. (a) Simplify the following function in SOP form using Quine MC-Cluskey method:
F (A, B, C, D)=∑m(1,2,3,5,6,7,8,9,12,13,15). [(CO1) (Analyze/IOCQ)]
(b) Realize the X-OR gate and AND gate using MUX 2:1. [(CO2) (Analyze/IOCQ)]

5 + (4 + 3) = 12

Group – C

4. (a) Explain how Shannon's Expansion Theorem enables:-
(i) Implementation of any Logic Function by Multiplexer.
(ii) Compression of Truth Table of a Function. [(CO2) (Remember/LOCQ)]
(b) For a 4 I/P Logic Function, Y = f(A, B, C, D), the Output is 0 when the Decimal Value equivalent to the value of the combination of 1 bit binary values of the I/P Variables is divisible by 4 (such as, for example, A=1, B=0, C=0, D=0, that is, ABCD = 1000 = $(1000)_2$ = $(8)_{10}$ = 8, 8 is divisible by 4, then the Output is 0) otherwise the Output is 1. Implement the Logic Circuit of the given function by a 8:1 Multiplexer. [(CO2) (Create/HOCQ)]
(c) Design the combined Logic Circuit of Full Adder-cum-Full Subtractor.
[(CO2) (Create/HOCQ)]

3 + 5 + 4 = 12

5. (a) Design and explain the operation of SRAM. [(CO6) (Understand/LOCQ)]
(b) Implement the following Boolean function using 8:1 MUX considering D as the input and A,B,C as selection lines: F(A,B,C,D)= AB' +BD +B'CD'.
[(CO2)(Analyze/IOCQ))]
(c) Design Full subtractor circuit using 4:1 Multiplexer. [(CO2) (Analyze/IOCQ)]

7 + 2 + 3 = 12

Group - D

6. (a) Draw the Logic Circuits and derive the Function Tables of S-R, D and J-K Flip Flops. [(CO3) (Analyze/IOCQ)]
   (b) What is Race Around Condition in Flip Flop? How is it eliminated? [(CO3) (Understand/LOCQ)]
   (c) Explain the difference between Combinational and Sequential Logic Circuits. [(CO3) (Remember/LOCQ)]

6 + 3 + 3 = 12

7. (a) Design a 4-Bit Asynchronous Up and Down Counter. [(CO3) (Analyze/IOCQ)]
   (b) Design of a synchronous MOD 6 counter using JK flip flops. [(CO3)/(Creative/HOCQ)]

2 + 10 = 12

Group – E

8. (a) Implement a 2-input NOR gate using CMOS inverter. [(CO5)(Analyze/IOCQ)]
   (b) Design and explain the operation of CMOS NOR Gate. [(CO5) (Analyze/IOCQ)]
   (c) Explain the point/points of Superiority of CMOS Logic over other Logic Families. [(CO5) (Understand/LOCQ)]

5 + 4 + 3 = 12

9. (a) Design a 4-Bit Flash Type Analog-to-Digital Converter. [(CO4) (Apply/IOCQ)]
   (b) When does a TTL circuit act as a current sink and source? [(CO5) (Remember/LOCQ)]
   (c) Design and explain the operation of CCD EEPROM. [(CO6) (Analyze/IOCQ)]

5 + 2 + 5 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	34.3%	37.5%	28.2%

Course Outcome (CO):

After the completion of the course students will be able to :-

1. Make use of the concept of Boolean algebra to minimize logic expressions by the algebraic method, K-map method, and Tabular method.
2. Construct different Combinational circuits like Adder, Subtractor, Multiplexer, De-Multiplexer, Decoder, Encoder, etc.
3. Design various types of Registers and Counters Circuits using Flip-Flops (Synchronous, Asynchronous, Irregular, Cascaded, Ring, Johnson).
4. Outline the concept of different types of A/D and D/A conversion techniques.
5. Realize basic gates using RTL, DTL, TTL, ECL, and CMOS logic families.
6. Relate the concept of Flip flops to analyse different memory systems including RAM, ROM, EPROM, EEROM, etc.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
IT	https://classroom.google.com/w/NDA1MjY0MDY2MTM3/tc/NDc1MTY0Njg3Mjcx
BACKLOG	https://classroom.google.com/c/NDc1MTY1OTI2NDky?cjc=2l56574