B.TECH/IT/3RD SEM/INFO 2102(BACKLOG)/2021

COMPUTER ORGANIZATION
(INFO 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which architecture involves both the volatile and the non volatile memory?
(a) Harvard architecture (b) Von Neumann architecture
(c) None of the mentioned (d) All of the mentioned

(ii) In instruction format, address of any data location is said to be
(a) function code (b) instruction code
(c) operand (d) logical code

(iii) The addressing mode which makes use of in-direction pointers is _____
(a) Indirect addressing mode (b) Index addressing mode
(c) Relative addressing mode (d) None of the above

(iv) The addressing mode, where you directly specify the operand value is _____
(a) Immediate (b) Direct
(c) Definite (d) Relative

(v) Booth's algorithm of multiplication is used for
(a) multiplication of signed 2's complement number
(b) multiplication of signed 1's complement number
(c) division of any number
(d) none of the above

(vi) Processor without structural hazard is
(a) Faster (b) Slower
(c) Have longer clock cycle (d) Have larger clock rate

(vii) In devices, controller is used for _____
(a) Buffering the data (b) Manipulate the data
(c) Calculate the data (d) Input the data

(viii) The BOOT sector files of the system are stored in _____
(a) Harddisk (b) ROM
(c) RAM (d) motherboard

(ix) The number successful accesses to memory stated as a fraction is called as _____
(a) Hit rate (b) Miss rate
(c) Success rate (d) Access rate

(x) The extra time needed to bring the data into memory in case of a miss is called as _____
(a) Delay (b) Propagation time
(c) Miss penalty (d) None of the mentioned.

Group- B

2. (a) Define Von-Neumann bottleneck? What is the solution of this? [(CO1)(Remember/LOCQ)]
(b) Explain with example why "Relative addressing" is very much popular in programming? [(CO1) (Understand/LOCQ)]
(c) Justify Computer organization comes after computer architecture. [(CO1)(Evaluate/HOCQ)]

(3 + 2) + 4 + 3 = 12

3. (a) Differentiate between "Indexed Address Mode" and "Base Register Address Mode". [(CO6)(Analyze/IOCQ)]
(b) X=(A*B)X(C/D)/E
Evaluate the above expression with the help of zero address, one address, two address and three address instructions. [(CO6) (Evaluate/HOCQ)]

4 + 8 = 12

Group - C

4. (a) Derive the working principle of Carry look Ahead Adder. [(CO5)(Create/HOCQ)]
(b) Explain biased exponent? Why it is required? [(CO4)(Understand/LOCQ)]
(c) Explain why 127 is subtracted after multiplying two floating point number with biased exponent? [(CO4)(Understand/LOCQ)]

4 + 4 + 4 = 12

5. (a) Multiply (-14) and (-8) applying Booth's multiplication algorithm. (CO4) (Understand/IOCQ)]
(b) Draw flowchart of Non Restoring type of Division algorithm. With the help of algorithm prove that both restoring and non restoring division are same. (CO4) (Understand/LOCQ)]

6 + (3 + 3) = 12

Group - D

6. (a) Compare and Contrast SRAM and DRAM. [(CO3) (Analyze/IOCQ)]
   (b) Evaluate how many 256 × 4 RAM chips are required to provide a memory capacity of 2048 bytes? Draw the interconnection diagram. [(CO3) (Evaluate/HOCQ)]

4 + (5 + 3) = 12

7. (a) Explain different types of locality of references in memory system. [(CO3) (Understand/LOCQ)]
   (b) According to the information, determine the number of bits of the subfields in the address for direct mapping, associative mapping and SAM cache schemes.
   Main memory size: 256 MB
   Cache memory size: 1 MB
   Address space of the processor: 256 MB
   Block size: 128 bytes
   There are 8 blocks in a set. [(CO3) (Evaluate/HOCQ)]

(2 × 3) + 6 = 12

Group - E

8. (a) Explain relative advantages and disadvantages of pipeline architecture over non pipeline architecture. [(CO1) (Understand/LOCQ)]
   (b) Discuss on different type of pipeline hazards. [(CO1) (Understand/LOCQ)]

6 + 6 = 12

9. (a) What is interrupt? Differentiate between interrupt and polling. [(CO1) (Analyze/IOCQ)]
   (b) Briefly explain the working principle of DMA. What is cycle stealing? [(CO3) (Understand/LOCQ)]

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	48.95%	20.83%	31.25%

Course Outcome (CO):

After the completion of the course students will be able to

CO1. Justify the necessity of using pipeline architecture over non pipeline architecture.
CO2. Compare between different page replacement algorithms.
CO3. Design memory unit with the help of decoder, multiplexer, and register.
CO4. Construct ALU considering basic arithmetical problems (addition, subtraction, multiplication, division) and logical problems.
CO5. Design 4 bit ripple carry adder and carry look ahead adder.

CO6. Formulate different solution strategy for different type of instructions.

*LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question

Department & Section	Submission Link
IT	https://classroom.google.com/c/NDU4NTkzMjUxNDQ2/a/NDc3NTI3MTQ4MjUx/details