COMPUTER ORGANIZATION
(INFO 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Cache memory is made upon
(a) Bipolar Semiconductor
(b) Unipolar semi conductor device
(c) Optical disk
(d) Magnetic storage.

(ii) The DMA transfer is initiated by _____
(a) Processor (b) the process being executed
(c) I/O devices (d) OS.

(iii) In a microprocessor the next instruction to be executed stored in
(a) Stack pointer (b) Accumulator
(c) Program counter (d) none.

(iv) MOV B, A is
(a) Immediate Addressing (b) Register Addressing
(c) Direct Addressing (d) Indirect Addressing Mode.

(v) "Delayed Branching" is related to
(a) pipeline hazard (b) pipeline remedy
(c) both (a) & (b) (d) none of (a), (b) and (c).

(vi) DVD writer is a
(a) semi random (b) serial
(c) random (d) non-serial access memory.

(vii) "Flops" and "MIPS" are related to the term speed of
(a) Processor (b) Primary memory
(c) both (a) & (b) (d) none of (a), (b) and (c).

(viii) For converting virtual address into physical address, the programs are divided into
(a) Pages (b) Frames (c) Segments (d) Blocks.

(ix) The BOOT sector files of the system are stored in
(a) Hard disk
(b) ROM
(c) RAM
(d) Fast solid state chips in the motherboard.

(x) How many address lines are needed to address each memory location in 2049 × 4 memory chip?
(a) 2 (b) 48 (c) 12 (d) 24.

Group – B

2. (a) Draw and explain Von-Neumann architecture. What is its drawback?

(b) What are the different types of instruction formats? Explain briefly.

(5 + 2) + 5 = 12

3. (a) What is the advantage of relative addressing mode over direct addressing mode? Explain with example.

(b) Evaluate the statement X = (A + B)*(C + D) using zero, one, two, three address instruction.

4 + (4 × 2) = 12

Group – C

4. (a) What is the drawback of ripple carry adder? Explain the working principle of carry look ahead adder.

(b) In which context Booth's multiplication Algorithm is suitable? Multiply (-8) with (4) with the help of Booth's multiplication algorithm.

(2 + 4) + (2 + 4) = 12

5. (a) Divide 19 by 7 using restoring type of division algorithm. What is biased exponent?

(b) How arithmetic and logic part are handled in ALU for different set of arithmetic and logic input? Explain with example.

(4 + 2) + 6 = 12

Group – D

6. (a) "Set Associative Mapping is combination of Associative Mapping and Direct Mapping Technique" — justify.

(b) Show the BUS connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip 512 × 8 bit size. Assume the CPU has 8 bit data bus and 16 bit address bus. Clearly specify generation of chip select signals.

6 + 6 = 12

7. (a) Calculate hit ratio for the following page references using LRU and frame size 5.
7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1
What is Belady's anomaly?

(b) According to the information, determine the number of bits of the subfields in the address for direct mapping, associative mapping and SAM cache schemes.
Main memory size: 256 MB
Cache memory size: 1 MB
Address space of the processor: 256 MB
Block size: 128 bytes
There are 8 blocks in a set.

(4 + 2) + 6 = 12

Group – E

8. (a) Calculate the speed up factor of a n stage pipeline. When the efficiency will be maximum?

(b) What is pipeline hazard? Briefly describe different hazard present in a pipeline.

(3 + 3) + (2 + 4) = 12

9. (a) What is interrupt? Differentiate between interrupt and polling.

(b) Briefly explain the working principle of DMA. What is cycle stealing?

(2 + 3) + (4 + 3) = 12