DIGITAL ELECTRONICS
(INFO 2101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The number of FFs required in a decade counter is _____
(a) 3 (b) 4 (c) 5 (d) 6.

(ii) How many flip–flops are needed to divide the input frequency by 64?
(a) 2 (b) 4 (c) 6 (d) 8.

(iii) A flip–flop circuit can be used for _____
(a) scaling (b) counting
(c) demodulation (d) modulation.

(iv) The minimum number of 2 input NAND gates required to realize half adder circuit are
(a) 3 (b) 4 (c) 5 (d) 6.

(v) How many full adder required to construct an m-bit parallel adder?
(a) m/2 (b) m-1 (c) m (d) m+1.

(vi) A MUX with its address bits generated by a counter operates as a
(a) parallel to serial converter (b) serial to parallel converter
(c) modified counter (d) modified MUX.

(vii) The term which can not be combined further in the tabular method are called
(a) Implicants (b) PI (c) EPI (d) SPI.

(viii) Data distributers are basically same as
(a) Decoder (b) Demultiplexer
(c) Multiplexer (d) Priority Encoder.

(ix) The logic family with both levels negative is
(a) TTL (b) ECL (c) CMOS (d) RTL.

(x) The 9's complement of the number 45 is
(a) 22 (b) 23 (c) 24 (d) 54.

Group – B

2. (a) Convert the following binary numbers into Gray code: (i) 1011 (ii) 1111.

(b) Reduce the following logic function using mapping the expression:
$F(w, x, y, z) = \sum m\ (0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$.

(c) Realize XOR function using AOI.

3 + 5 + 4 = 12

3. (a) Find the possible bases in arithmetic operation
(i) 51/3 = 13 (ii) $(292)_{10} = (565)_R$.

(b) Given that, $AB' + A'B = C$. Prove: $AC' + A'C = B$.

(c) Simplify the following logic function using Karnaugh Map
$F(w, x, y, z) = \sum m\ (1, 5, 6, 7, 11, 12, 13, 15)$.

4 + 3 + 5 = 12

Group – C

4. (a) Implement full adder circuit using a decoder and OR gate.

(b) Implement the following logic function using (8 × 1) MUX
$F(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 10, 11, 14, 15)$

7 + 5 = 12

5. (a) Explain the working principle of BCD adder with suitable diagram.

(b) Explain the operation principle of 2 bit magnitude comparator circuit.

7 + 5 = 12

Group – D

6. (a) Design a MOD – 10 counter.

(b) Explain J-K flip-flop using proper logic diagram and truth table.

8 + 4 = 12

7. Design a sequence detector that produces an output 1 whenever the sequence 10101 is detected.

12

Group – E

8. (a) Explain the operation principle of successive approximation type ADC with suitable diagram.

   (b) The logic levels used in a 4 bit R-2R ladder DAC are, logic1 = 5 V and logic0 = 0 V. Find the output voltage for input 0010.

7 + 5 = 12

9. Write short notes on following (any two):
   (i) Flash ADC (ii) Logic family (iii) Dual Slope ADC (iv) TTL.

(6 + 6) = 12