DIGITAL LOGIC
(ECEN 2104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) A two input XOR gate can be used as an inverter when one of the inputs is at logic?
(a) 0 (b) 1 (c) None (d) Ground.

(ii) The excess-3 code for decimal 279 is
(a) 010110101100 (b) 011010111111
(c) 001001111100 (d) 001010101001.

(iii) Which device changes parallel data to serial data
(a) counter (b) multiplexer
(c) demultiplexer (d) flip flop.

(iv) If (24 + 17) = 40 then the base of the numbers is
(a) 5 (b) 6 (c) 9 (d) 11.

(v) When 567432.15 in Octal is converted to Hex it has a value of
(a) BBC68.87 (b) 2EF1A.34
(c) ABC68.23 (d) 3EF1B.24.

(vi) An n-stage ripple counter can count up to power?
(a) 2^n (b) $2^n - 1$ (c) n (d) $2^{(n-1)}$

(vii) Which logic gate family uses the minimum power
(a) TTL (b) CMOS (c) ECL (d) DTL.

(viii) The number of flip flops needed for a Mod 7 counter are
(a) 7 (b) 5 (c) 3 (d) 1.

(ix) Race around condition is avoided using
(a) Look ahead carry generator (b) J-K flip flop
(c) Edge triggered flip flop (d) Faster gates.

(x) Gray Code of $(110101)_2$ is
(a) 101111 (b) 100110 (c) 111010 (d) 101011.

Group - B

2. (a) Simplify algebraically the following Boolean expression: (A+C+D).(A+C+D').(A+C'+D)(A+B')

(b) Express the following function F = B'D + A'D + BD in SOP and POS form.

(c) Determine Prime Implicants (PI), and Essential PIs from the function F(A,B,C,D) = ∑(0,1,3,5,7,11,14,15).

4 + 4 + 4 = 12

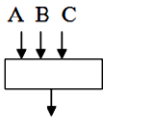
3. (a) Simplify the given Boolean expression using Quine-McCluskey procedure *f(A,B,C)= ∑m(0,1,2,5,6,7)*.

(b) Implement full-adder circuit using decoder and OR gates.

6+6=12

Group - C

4. (a) A Three input BMB Function whose characteristics with K-map are shown below has been mass produced by an unfortunate company. Experimental evidence showed that the input combinations 101 and 010 cause the gate to "explode". Your task is to determine whether the gate is completely useless or can be externally modified so that it may be efficiently used to implement any switching function without causing explosion.



A \ BC	00	01	11	10
0	1	1	0	1
1	0	1	0	0

BMB(A ,B, C)

(b) An 8×1 multiplexer has inputs A, B, C connected to selection lines s_2, $s_1$and s_0 respectively. The data inputs are as follows $I_1=I_2=I_7=0$; $I_3=I_5=1$; $I_0=I_4=D$ and $I_6=D'$. Determine the Boolean function F(A,B,C,D) implemented by the multiplexer.

6 + 6 = 12

5. (a) Design a four-bit binary parallel adder circuit using full-adder circuit blocks.

(b) Design a *2*-bit magnitude comparator circuit.

6 + 6 = 12

Group - D

6. (a) Design a RS latch using NAND gates. What is its indeterminate state? Design a D latch with RS latch and explain with a function table how the indeterminate state is avoided.

(b) We have input X and Y and output A of a system with a D flop flop. The system is a clocked sequential circuit with equation A(t + 1) = X xor Y xor A(t). Implement the system with excitation and state tables.

(2 + 1 + 3) + 6 = 12

7. (a) Design an asynchronous counter that goes through the states 0-1-2-3-4-0.

(b) Convert T flip-flop to D flip-flop.

6 + 6 = 12

Group - E

8. (a) Implement the XOR gate using CMOS logic circuit.

(b) Design a NAND Gate using a RTL logic circuit.

6 + 6 = 12

9. (a) For an 8 bit DAC (Digital to Analog Converter), calculate the values of LSB, and full scale output voltage for the range of 0 to 10V.

(b) A circuit accepts a three bit number and generates an output binary number equal to the square of the input number. Design the combinational circuit using a 8×4 ROM for this set up.

6 + 6 = 12