B.TECH/IT/3RD SEM/INFO 2102/2018
COMPUTER ORGANIZATION
(INFO 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which architecture involves both the volatile and the non- volatile memory?
(a) Harvard architecture (b) Von Neumann architecture
(c) None of these (d) Both of these.

(ii) The addressing mode which makes use of in-direction pointers is _____
(a) indirect addressing mode (b) index addressing mode
(c) relative addressing mode (d) none of the above.

(iii) The addressing mode, where you directly specify the operand value is _____
(a) immediate (b) direct (c) definite (d) relative.

(iv) Booth's algorithm of multiplication is used for
(a) multiplication of signed 2's complement number
(b) multiplication of signed 1's complement number
(c) division of any number
(d) none of the above.

(v) "Delayed Branching " is related to
(a) pipeline hazard (b) pipeline remedy
(c) both (a) and (b) (d) none of these.

(vi) Each interaction between CPU and I/O module involves:
(a) bus arbitration (b) bus revolution
(c) data bus (d) control signals.

(vii) The technique used to store programs larger than the memory is _____
(a) overlays (b) extension registers
(c) buffers (d) both extension registers and buffers.
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(viii) Which architectural scheme has a provision of two sets for address and data buses between CPU and memory?
(a)Harvard architecture (b) Von-Neumann architecture
(c) Princeton architecture (d) all of the above.

(ix) In case of, zero-address instruction method the operands are stored in _____
(a) registers (b) accumulators
(c) pushdown stack (d) cache.

(x) The extra time needed to bring the data into memory in case of a miss is called as _____
(a) delay (b) propagation time
(c) miss penalty (d) none of the mentioned.

Group – B

2. (a) Draw and explain Von-Neumann architecture. (Explain each component).

(b) Why is "relative addressing" very much popular in programming? Explain with example.

8 + 4 = 12

3. (a) Differentiate between "Indexed Address Mode" and "Base Register Address Mode".

(b) X =(A * B) * (C / D)/E Write down the zero-address, one-address, two - address and three - address instructions for the above expression.

4 + 8 = 12

Group – C

4. (a) Prove that final carry in carry look ahead adder is dependent only on the carry generated in first adder.

(b) What is biased exponent? Why is it required? Why is 127 subtracted after multiplying two floating point numbers with biased exponent?

6 + (2+2+2) = 12

5 .(a) Multiply -13 and 7 with the help of Booth is multiplication algorithm.

(b) Draw the flow chart of restoring type of division algorithm. Divide 8 by 3 with the help of non-restoring type of division algorithm.

6 + (3 + 3) = 12

Group – D

6. (a) What is memory interleaving? Explain the different types of memory interleaving.

(b) Show the bus connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip of size 256 × 8 bits. Assume the CPU has 8- bit data bus and 16-bit address bus.

(c) What are write-back and write-through policies in cache memory?

(2 + 3) + 5+ 2 = 12

7. (a) What is the limitation of direct mapped cache? Explain with an example how it can be improved in set-associative cache.

(b) According to the information, determine the number of bits of the subfields in the address for direct mapping, associative mapping and SAM cache schemes.
Main memory size: 256 MB
Cache memory size: 1 MB
Address space of the processor: 256 MB
Block size: 128 bytes
There are 8 blocks in a set.

(2 + 4) + 6 = 12

Group – E

8. (a) Explain relative advantages and disadvantages of pipeline architecture over non pipeline architecture.

(b) Discuss the different types of pipeline hazards.

6 + 6 = 12

9. (a) Compare RISC and CISC. Explain interrupt initiated I/O transfers with proper diagram.

(b) What is interrupt? Differentiate between vectored and non-vectored interrupt?

(6) + (2 + 4) = 12