DIGITAL ELECTRONICS
(ECEN 2002)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Which one of the following is a weighted code?
(a) 2421 (b) Excess-3
(c) Gray (d) None of these.

(ii) The Boolean expression $AB + A\bar{B} + \bar{A}C + AC$ is independent of the Boolean variable
(a) A (b) B (c) C (d) none of the above.

(iii) The 2's complement representation of $(-19)_{10}$ is
(a) 101100 (b) 101110
(c) 101101 (d) none of the above.

(iv) The minimum number of NAND gates required to implement the Boolean function $(A + A\bar{B} + A\bar{B}C)$ is
(a) 1 (b) 4 (c) 7 (d) 0.

(v) The fastest ADC is
(a) Dual slope (b) SAR
(c) Counter (d) none of these.

(vi) An n-bit parallel adder consists of
(a) (n+1) full-adders (b) (n-1) full-adders
(c) n full-adders (d) 2n full-adders.

(vii) Which of the following uses the least power?
(a) TTL (b) ECL
(c) CMOS (d) All use same power.

(viii) If $(2X)_8 = (34)_X$, then find the value of X.
(a) 6 (b) 12 (c) 4 (d) 8.

(ix) Don't care condition is
(a) Logic 0
(b) Logic 1
(c) Logic 0 or Logic 1 where ever required
(d) none of the above.

(x) Race around condition is avoided using
(a) J-K flip flop (b) Look ahead carry generator
(c) Edge triggered flip flop (d) Faster gates.

Group – B

2. (a) Differentiate between combinational logic circuit and sequential logic circuit.

(b) Minimize the following Boolean function and implement the circuit using basic gates:
F(A, B, C, D) = $\sum_m(1, 3, 4, 5, 9, 10, 11) + \sum_d(6, 8)$.

4 + 8 = 12

3. (a) Why NAND and NOR gates are known as Universal gates? Justify your answer.

(b) Simplify the following function by means of tabulation method:
F(A, B, C, D) = $\sum_m(0, 1, 4, 7, 9, 11, 13) + \sum_d(3, 5)$.

5 + 7 = 12

Group – C

4. (a) Construct a 4:1 line multiplexer using three 2:1 line multiplexers only.

(b) Implement the function f (a, b, c) = $\sum m$ (1, 3, 5, 6) using a 4:1 line Multiplexer.

(c) Implement full-adder circuit using decoder and OR gates.

5 + 3 + 4 = 12

5. (a) Design a BCD adder that adds two 4 bit BCD numbers.

(b) Construct a 5-to-32 decoder with four 3-to-8 and one 2-to-4 decoder (use block diagram of decoder).

6 + 6 = 12

Group – D

6. (a) Write down the characteristic equation of J-K flip-flop.

(b) What advantage does a J-K flip-flop have over an S-R flip-flop?

(c) Realize D flip-flop using T flip-flop.

2 + 3 + 7 = 12

7. (a) Design a synchronous decade up counter using J-K flip flop.

(b) Design a bidirectional shift register using D flip-flops and explain its operation.

6 + 6 = 12

Group – E

8. (a) Explain a successive approximation A/D converter with proper circuit diagram. What will be the conversion time of such a ADC which uses 2 MHz clock and a 5 bit binary ladder using 8V reference?

(b) Which is the fastest ADC? Explain its operation.

7 + 5 = 12

9. (a) Design a basic 2 input TTL NAND gate and explain.

(b) For a R-2R ladder 4 bit DAC with R = 10KΩ and V_R = 10V, find out the feedback resistance R_f of the OPAMP for
(i) analog output of 6V for a binary input of 1000.
(ii) full scale output voltage of 12V.

6 + 6 = 12