B.TECH / ECE /5TH SEM/ ECEN 3103/2017
MICROELECTRONICS & ANALOG VLSI DESIGN
(ECEN 3103)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) According to Moore's Law, Number of Transistor per chip gets doubled in
(a) 18 Months (b) 12 Months (c) 24 Months (d) 30 Months.

(ii) Flat - Band voltage is defined as the applied gate voltage such that there is
(a) no band bending in the semiconductor at the oxide –semiconductor interface.
(b) no band bending in the oxide at the oxide – semiconductor interface
(c) zero net space charge in the semiconductor at the oxide – semiconductor interface
(d) both (a) & (c).

(iii) Value of "Lambda" in 130nm Process Node is
(a) 130nm (b) 100nm (c) 90nm (d) 65nm.

(iv) The rms voltage of the sampled noise in a sampling circuit is
(a) $(KT/C)^{1/2}$ (b) $(KT/C)^{-1/2}$ (c) (KT/C) (d) $(KT^{1/2}/C)$.

(v) Saturation Region of Ideal MOS Transistor can be modelled as
(a) Resistance (b) Capacitance
(c) Current Source (d) Voltage Source.

(vi) One of the primary disadvantages of the switched capacitor circuit is
(a) Overlapping clock (b) Nonoverlapping clock
(c) Current Source (d) Voltage Source.

(vii) 3D Transistor is created using _____ Fabrication Process.
(a) Planner (b) SOI (c) FINFET (d) none of Above.

(viii) CMRR for a perfectly Matched Differential Amplifier Circuit is
(a) zero (b) one (c) infinite (d) none of Above.

(ix) For amplifier operation, the push – pull inverting CMOS amplifier should have
(a) PMOS in saturation, NMOS in non-saturation
(b) PMOS in non - saturation, NMOS in saturation
(c) PMOS and NMOS both in saturation
(d) PMOS and NMOS both in non-saturation.

(x) The speed of growth of Si crystals in CZ process is determined by
(a) ambient temperature
(b) the number of sites on the face of the crystal
(c) the specifics of heat transfer at the interface
(d) both (b) & (c)

Group - B

2. (a) Explain the phenomenon of channel length modulation of the MOSFET and correlate this with the different regions of the drain characteristics of the MOSFET.

(b) Identify the constructional difference between depletion type and enhancement type MOSFET. Explain the key phenomenon behind the principle of operation of the enhancement type MOSFET as a switch.

6 + (2 + 4) = 12

3. (a) What is Constant Voltage Scaling and Constant Field Scaling?

(b) Which Scaling is more popular and why?

(c) Explain Short Channel Effects.

4 + 3 + 5 =12

Group – C

4. (a) Explain Photo Lithography.

   (b) Write short note on Oxidation and Diffusion.

   (c) What is difference between Lambda and Micron Rules.

4 + (3 + 3) + 2 = 12

5. (a) State the purpose of ion implantation process.

   (b) Briefly describe the n-well fabrication process.

(2 + 10) = 12

Group – D

6. (a) Explain the model for a non – ideal MOS switch. Mention the mechanisms during MOS transistor operation that introduce error at the instant the switch turns off.

   (b) Explain the channel charge injection phenomenon and briefly discuss any one of the techniques adopted for charge injection cancellation.

(5 + 1) + (3 + 3) = 12

7.(a) Draw Small Signal low frequency model for NMOS.

   (b) How MOS can be used as Diode?

   (c) Derive the expressions for DC and AC resistances of MOS diode.

   (d) Explain Supply Voltage Divider Circuit using NMOS Transistors.

(3 + 3 + 3 + 3) = 12

Group – E

8. (a) Explain how NMOS can be used as Current Sink.

   (b) Explain Basic Current Mirror Circuit.

   (c) Explain CMOS bandgap reference circuits.

(3 + 4 + 5) = 12

9. (a) Emulate the resistor equivalent of a parallel switched capacitor circuit. For this configuration, if the clock frequency is 100 KHz, find the value of the capacitor C that will emulate a 1MΩ resistor.

   (b) Explain the sample and hold capabilities of a sampling circuit.

(6 + 2) + 4 = 12