B.TECH/CSE/5TH SEM/AEIE 3105/2017
MICROPROCESSORS & MICROCONTROLLERS
(AEIE 3105)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Among the followings which signal has the lowest priority of 8085?
(a) INTR (b) RST 7.5 (c) TRAP (d) RST5.5.

(ii) To make the accumulator content double which of the following instructions requires to execut in 8085?
(a) RLC (b) RAL (c) XRAA (d) None of the above.

(iii) Which of the following is an invalid instruction?
(a) NOP (b) XCHG D (c) ADC M (d) LHLD 1234H.

(iv) The number of address lines required for 16KB memory chip is
(a) 13 (b) 14 (c) 15 (d) 16.

(v) In 8086 how many flag bits are there in flag register?
(a) 16 (b) 9 (c) 5 (d) 8.

(vi) PSW in 8085 microprocessor is
(a) 8 bits (b) 16 bits (c) 4 bits (d) 32 bits.

(vii) The vector address corresponding to software interrupt command RST 7 in 8085 microprocessor is
(a) 0017H (b) 0027H (c) 0038H (d) 0700H.

(viii) What will be the starting physical address of CS if CS=2345H and IP=1000H?
(a) 23450H (b) 24450H (c) 12345 H (d) 2345H.

(ix) If CWR port address is 1F H, what will be the address of Port A of that 8255A?
(a) 1CH (b) 20H (c)10H (d) Not possible to determine.

(x) In 8051 microcontroller, index addressing mode is represented by the instruction _____.
(a) MOVC A@A+DPTR (b) MOVX @DPTR,A
(c)MOVX A@DPTR (d)MOVXA@R_0.

Group – B

2. (a) Draw the timing diagram for the instruction ***(any one)*** from the following:
i) ADI 37H ii) MOV M,C iii) IN 7DH.

(b) Describe the significance of the following pins of 8085A microprocessor ***(any three):***
TRAP, ALE, $\overline{\text{RESET IN}}$, IO/$\overline{\text{M}}$, $\overline{\text{WR}}$, HLDA.

(c) Explain the significance of multiplexed address data bus in 8085.

6 + 3 + 3 = 12

3. (a) What do you mean by conditional and unconditional branch control instructions? Give example.

(b) Write down an assembly language program using 8085μp to take ten numbers in any array. Check the even and odd numbers from that array one by one. Add all the even numbers and store the result in C200H, C201H.

(c) Specify the content of A, B and flag register status for S, Z and CY for the following program.
MVI A, 4AH
SUI 40H
STC
ANA B
HLT

(d) Explain the operation of different interrupts of 8085 microprocessors with the help of diagram.

3 + 3 + 3 + 3 = 12

Group – C

4. (a) What do you mean by pipelined architecture? How can it be implemented in 8086?

(b) Explain the concept of segmented memory. What are its advantages?

(c) Explain with diagram how a 20 bit physical address is generated in 8086 microprocessor. If address of CS = 4000H and address of IP = 1000H. Find the starting and ending address of CS.

(2 + 2) + (2 + 2) + (2 + 2) =12

5. (a) Explain the function of the following signals of 8086 (***any four***).
ALE, DT/$\overline{R}$, $\overline{DEN}$, $\overline{LOCK}$, $\overline{TEST}$, MN/$\overline{MX}$, $\overline{BHE}$, RQ/$\overline{G}$T

(b) With a diagram, explain the process of demultiplexing of address and data buses of 8086 microprocessor.

(c) Write down the differnt interrupts of 8086 microprocessor.

6 + 4 + 2 = 12

Group – D

6. (a) Write down the addressing modes of the following instructions
(i) MOV A, @A+DPTR (ii) MOVX @DPTR,A
(iii) MOVX R_0,#45H (iv) MOV A, @R_0
What is the difference between CY and OV flag?

(b) Explain the operation of the following pins:
i) TXD ii) XTAL2 iii) $\overline{EA}$ iv) $\overline{PSEN}$

(4 + 2) + 6 = 12

7. (a) What is the difference between internal and external memory 8051 microcontroller? Write down the bit pattern of PCON register of 8051.

(b) Explain the operation of timer of MODE 1 of 8051 microcontroller How many numbers of instructions are there in PIC 16F877?

(3 + 3) + (3 + 3) = 12

Group – E

8.(a) What is BSR Mode in 8255A? Draw control word pattern for BSR Mode.

(b) Write short notes on (***any one):***
DMA Controller, USART 8251

(c) Explain ICW1 and ICW2 of 8259.

(1 + 2) + 5 + 4 = 12

9. (a) Compare Memory mapped I/O and I/O mapped I/O.

(b) An 8k × 8 RAM is interfaced with 8085A using a NAND gate. Calculate the final address of the chip if initial accessible address is 4000H.

(c) Explain with a diagram how INTR signal is generated by 8255A, when Port A/B is acting as I/P port in interrupt I/O mode.

3 + 3 + 6 = 12