B.TECH / CSE /3RD SEM/ ECEN 2104/2017
DIGITAL LOGIC & COMPUTER ORGANIZATION
(ECEN 2104)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The _____ format is usually used to store data in a computer system.
(a) BCD (b) Decimal (c) Hexadecimal (d) Octal.

(ii) NAND and NOR logic gates are also called
(a) Main Gates (b) Universal Gates
(c) Principal Gates (d) Head Gates.

(iii) The Boolean expression X * (Y + Z) = (X * Y) + (X * Z) holds true by the
(a) Distributive law (b) Associative law
(c) law of Identity (d) law of compliments.

(iv) With respect to the input lines of a decoder, each of the output lines represents a corresponding
(a) Voltage Line (b) Number Tagged Wire
(c) Maxterm (d) Minterm.

(v) If a function is shown as F(A, B, C, D) =∑ (1,2,4,5,8,9,10,11,15), then its compliments F' is given by.
(a) F'=∑ (1,2,4,5,8,9,10,11,15), (b) F'= ∑ (1,2,4,5,8,9,10,11,15)
(c) F'= ∑ (0,3,6,7,12,13,14), (d) F' =∑ (0,3,6,7,8,9,10,11,15) .

(vi) A Decoder with an enable input represents a functional
(a) Encoder (b) Multiplexer
(c) Comparator (d) Demultiplexer.

(vii) (x*y)*z=x*(y*z) is the
(a) Commutative property (b) Inverse property
(c) Identity element (d) Associative property.

(viii) The binary equivalent of the Gray code 11100 is
(a) 10111 (b) 00111 (c) 01011 (d) 10101

(ix) Between input and output lines the function of tristate buffer is to
(a) connect or isolate (b) find one 's compliment
(c) compliment the logic (d) find two's compliment.

(x) During transfer of data between the processor and memory we use _____
(a) Cache (b) TLB (c) Buffers (d) Registers.

Group - B

2. (a) The quadratic equation $x^2 - 11x + 22 = 0$ has solutions x = 3 and x = 6. Find the base of the numbers.

(b) Simplify T(x,y,z) = (x + y) (x + yz) + x'y' + x'z'

(c) Given AB' + A'B = C show that AC' + A'C = B.

4 + 4 + 4 = 12

3. (a) Determine the canonical sum-of-product representations of the function: f (x,y,z) = z + (x' + y) (x + y').

(b) The main stairway in a block of fiats has three switches for controlling the lights. Switch A is located at the top of the stairs, switch B is located halfway up the stairs and switch C is positioned at the bottom of the stairs. Design a logic network to control the lights on the staircase.

(c) Prove A XOR B = A' XOR B'.

4 + 5 + 3 = 12

Group - C

4. (a) Design a single bit full adder using a Decoder and OR gates.

(b) Determine the function f(A,B,C,D) = ∑ (0, 1, 3, 4, 8, 9, 15) using a 8 to 1 Mux.

(c) Use Booth's Algorithm to Multiply (-5) × (6) and obtain result.

4 + 4 + 5 = 12

5. (a) Design a 4 bit Adder Subtractor circuit using logic gates.

(b) A 8 to 1 MUX is used to implement a function F(A,B,C,D). It has inputs A, B, C connected to selection lines S2, S1, and S0. The data inputs I0 to I7 are as follows. I0 = I1 = I5 = D, I2 = D', I6 = I7=1, I3=I4=0. Determine the function F(A,B,C,D).

(c) Design a 4 bit BCD adder and discuss why you add 6.

4 + 4 + 4 = 12

Group – D

6. (a) Design a RS Flip Flop with NAND gates, and state with truth tables what is the prohibited state. Mention how to overcome it. What is a race condition in J - K Flip Flop ? How do you overcome it?

(b) Design an synchronous counter using J-K flip flops, which shall count from 000, 010, 011,101,110 and back to 000 state.

(2 + 1 + 2 + 1) + 6 = 12

7. (a) (i) Explain the basic concepts of a Finite State machine.
(ii) Distinguish between Mealy and Moore machines

(b) (i) Design a BCD counter with JK flip-flops.
(ii) Distinguish between a register and a latch.

(3 + 3) + (3 + 3) = 12

Group – E

8. (a) Classify the three categories of digital circuits using MOSFET. What is an active load?

(b) Describe working operation of NMOS inverter with circuit diagram and waveform.

(c) Describe a two input NOR gate using N-type MOSFET.

(3 + 1) + 4 + 4 = 12

9. (a) (i) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
(ii) Distinguish between SRAM and DRAM.

(b) A combinational circuit is defined by the functions:
$F1(A,B,C) = \sum(3,5,6,7)$
$F2(A,B,C) = \sum(0,2,4,7)$
Implement the circuit with a PLA having three inputs, four product terms, and two outputs.

(4 + 2) +6 = 12