(vii) Which of the following types of instructions are useful in handling sparse matrices in vector processing applications?
(a) Vector – Scalar instruction (b) Masking instruction
(c) Vector – memory instruction (d) None of these.

(viii) The prefetching is a solution for
(a) data hazard (b) structural hazard
(c) control hazard (d) none of these.

(ix) Which of the following is an example of 2-dimensional topologies in static network?
(a) Mesh (b) $3C_3$ Network
(c) Linear Array (d) None of these.

(x) Stride in vector processor is used to
(a) differentiate different data types (b) differentiate registers
(c) differentiate different data (d) none of the above.

Group – B

2. Consider the following reservation table. Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline? Find out simple cycle, greedy cycle and MAL. What are the bounds on MAL?

	1	2	3	4
S1	X			X
S2		X		
S3			X	

(2 + 4 + 4 + 2) = 12

3. (a) Explain how multiplication speed is increased using carry save adder instead of ripple carry adders.

(b) Draw the tree that results in multiplying two 5 bit numbers using CSA' s.

(c) Using a schematic diagram explain the floating point adder function.

(d) Explain various type of hazards with example.

(e) What is data forwarding?

2 + 3 + 3 + 3 + 1 = 12

Group – C

4. (a) Draw the diagram of a 8 × 8 Omega Network built with 2 × 2 switching elements.

(b) Show the switching setting for routing a message from node 001 to node 100 and from node 011 to node 101 simultaneously. Does blocking exist in this case?

6 + (3 + 3) = 12

5. (a) Explain Multistage implementation of a Cube Network with a suitable diagram.

(b) Implement data routing logic of SIMD architecture to compute

$$s(k) = \sum_{i=0}^{k} A_i \text{ for } k = 0, 1, 2 \ldots N-1.$$

(c) Why do we need masking mechanism in SIMD array processors?

4 + 5 + 3 = 12

Group – D

6. (a) State and explain Amdahl's law.

(b) How does Amdahl's Law & Gustafson's Law differ with respect to machine size and problem size?

(c) Consider the un-pipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from pipeline?

(d) What is locality of reference? Differentiate between temporal and spatial locality.

(2 + 3) + 2 + 3 + (1 + 1) = 12

7. (a) Develop $3^2 \times 4^2$ delta network.

(b) A 50 MHz processor was used to execute a program with the following instruction mix and clock cycle counts:

Instruction Type	Instruction Count	Clock Cycle Count
Integer Arithmatic	50000	2
Data Transfer	70000	3
Floating point arithmetic	25000	1
Branch	4000	2

Calculate the effective CPI, MIPS rate and execution time for this program.

(c) What is the significance of interconnection network in multiprocessor architecture?

4 + 5 + 3 = 12

Group – E

8. (a) What is meant by the cache miss penalty? Briefly discuss "early restart" technique to reduce miss penalty.

(b) Briefly describe cache coherence problem with an example. Suggest one software protocol for this.

(c) Compare between UMA & NUMA architectures.

(2 + 3) + (3 + 2) + 2 = 12

9. (a) With simple diagram explain the data flow architecture. How does it differ from control flow architecture? Draw dataflow graph for the following set of instructions

1. P = X + Y
2. Q = P ÷ Y
3. R = X × P
4. S = R − Q
5. T = R × P
6. U = S ÷ T

(b) Draw the various systolic array configurations.

(4 + 2 + 4) + 2 = 12

COMPUTER ARCHITECTURE
(CSEN 2203)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Cache memory works on the principle of
(a) locality of data (b) locality of reference
(c) locality of memory (d) locality of reference & memory.

(ii) Memory access in RISC architecture is limited to instructions
(a) CALL and RET (b) PUSH and POP
(c) STA and LDA (d) MOV and JMP.

(iii) Given that 5 functional units which operate in each of 5 cycles and are as follows:10ns, 8ns, 10ns, 10ns, 7ns. Assuming pipelining adds 1 ns of overhead, speedup in pipelining is
(a) 45 (b) 1.1 (c) 10 (d) 4.1.

(iv) A computer with cache access time of 40ns and hit ratio of 0.8 and regular memory has an access time of 100ns. What is the effective memory access time of CPU?
(a) 52ns (b) 60ns (c) 70ns (d) 80ns.

(v) Systolic Array can be thought of as an example of which of the following architecture?
(a) SISD (b) SIMD (c) MISD (d) MIMD.

(vi) The number of cycles required to complete n tasks with k stage pipeline is
(a) k + n - 1 (b) k (c) nk + 1 (d) none of these.