DIGITAL ELECTRONIC CIRCUITS
(AEIE 2201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

   (i) The range of positive numbers for n-bit signed binary number system is
   (a) 0 to 2^n-1 (b) 1 to 2^n-1
   (c) 1 to 2^n+1 (d) 0 to 2^n+1.

   (ii) r' s complement of a number 'N' having 'n' digit is
   (a) r^n - N (b) $(r-1)^n$-N
   (c) $(r+1)^n$-N (d) none of the above.

   (iii) A 3 bit subtractor circuit requires _____.
   (a) two full subtractor and two half subtractor
   (b) three full subtractor
   (c) two full subtractor and one half subtractor
   (d) one full subtractor and two half subtractor.

   (iv) When simplified with Boolean Algebra (x + y)(x + z) simplifies to
   (a) x (b) x + x(y + z)
   (c) x(1 + yz) (d) x + yz.

   (v) Propagation delay of a logic gate can be measured by
   (a) crystal oscillator (b) ring counter
   (c) ring oscillator (d) none of the above.

   (vi) Programmable Array Logic (PAL) consists of
   (a) Programmable AND and OR array
   (b) Programmable AND and fixed OR array
   (c) Programmable OR and fixed AND array
   (d) Fixed AND and OR array.

(vii) Decimal equivalent of the fractional octal number 2071.31 is
(a) 1024.625 (b) 201.5009
(c) 1081.3906 (d) 0.1099

(viii) How many flip-flops are required to make a MOD-33 binary counter?
(a) 15 (b) 6 (c) 5 (d) 30.

(ix) The terminal count of a typical modulous-15 binary counter is _____
(a) 1000_2 (b) 1110_2 (c) 1011_2 (d) 1101_2.

(x) A T- flip-flop with T = 1 has a 10 kHz clock input. The Q output is
(a) a 5 kHz square wave (b) constantly HIGH
(c) a 20 kHz square wave (d) a 10 kHz square wave.

Group – B

2. (a) Realize (i) an AND gate by using NOR gate.
(ii) an OR gate by using only NAND gate.

(b) Convert $(7414.2745)_8 = (???)_{16}$

(c) What is the difference between combinational and sequential circuits?

(d) Design a full adder circuit using 8:1 multiplexer.

(1 + 1) + 2 + 2 + 6 = 12

3. (a) Realize a 16:1 multiplexer by using 4:1 multiplexer.

(b) Implement the logic function Y(A, B, C, D) = ∑m(0, 3, 4, 5, 7, 9, 12, 13) by using 8:1 multiplexer.

4 + 8 = 12

Group – C

4. (a) Minimize the logic function Y(A, B, C, D) = ∑m(1, 3, 4, 5, 9, 11, 14, 15) + ∑d(2, 6, 7, 8) by using Karnaugh map.

(b) Design a J-K flip flop with truth table by using only NAND gates.

8 + 4 = 12

5. (a) "A –ve edge trigerred D flip-flop can work as master-slave flip-flop" – explain.

(b) Design a MODULO-16 synchronous counter and explain with output waveforms.

6 + 6 = 12

Group – D

6. (a) Design a ripple counter to start the count at 2 and stop the count at 7 and start the count again from zero.

(b) Give the comparison between synchronous and asynchronous counters.

8 + 4 = 12

7. (a) Write short note on Johnson counter.

(b) Implement the given functions using programmable logic array (PLA)
X(a, b, c) = $\sum m(0, 3, 4)$, Y(a, b, c) = $\sum m(3, 4, 5, 7)$.

4 + (4 + 4) = 12

Group – E

8. (a) Compare between logic families: TTL, ECL, and CMOS.

(b) Write short notes on Flash type ADC and Binary weighted DAC.

6 + (3 + 3) = 12

9. (a) Implement the following logic functions by using PROM.
W = $\sum n(0, 2, 4, 6, 9)$, X = $\sum m(0, 1, 3, 7, 9)$, Y = $\sum m(2, 4, 6, 7, 12)$

(b) Design a NAND gate using CMOS logic.

7 + 5 = 12