

**COMPUTER ORGANIZATION AND ARCHITECTURE
(CBS2202)**

Time Allotted : 2½ hrs

Full Marks : 60

Figures out of the right margin indicate full marks.

*Candidates are required to answer Group A and
any 4 (four) from Group B to E, taking one from each group.*

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve:

12 × 1 = 12

Choose the correct alternative for the following

- (i) In which addressing the simplest addressing mode where an operand is fetched from memory is _____:
 - (a) Immediate addressing
 - (b) Direct addressing
 - (c) Register addressing
 - (d) Indirect addressing
- (ii) If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associativemapping. Then each word of cache memory shall be
 - (a) 11 bits
 - (b) 21 bits
 - (c) 16 bits
 - (d) 20 bits
- (iii) There are five segments and eight tasks in one pipeline processing. Determine the required time (in clock cycles) to complete all the operations.
 - (a) 13
 - (b) 12
 - (c) 11
 - (d) 10
- (iv) A Stack-organised Computer uses instruction of
 - (a) Indirect addressing
 - (b) Two-addressing
 - (c) Zero addressing
 - (d) Index addressing
- (v) The disadvantage/s of the hardwired approach is _____
 - (a) It is less flexible
 - (b) Less flexible & cannot be used for complex instructions
 - (c) It cannot be used for complex instructions
 - (d) It is costly
- (vi) The main memory is 4K x 9 and cache memory is 256 X 9 in associative mapping. How many octal digits are required to express data?
 - (a) 6
 - (b) 4
 - (c) 9
 - (d) 3
- (vii) The addressing mode used in an instruction of the form ADD X Y, is
 - (a) Absolute
 - (b) indirect
 - (c) index
 - (d) none of these

- (viii) "Data Forwarding" (or Bypassing) is specifically used to resolve which of the following?
 (a) WAW hazards (b) WAR hazards
 (c) RAW hazards (d) Branch penalties
- (ix) In arithmetic pipeline, what is correct sequence of the sub-operations that are performed in the four segments which are? (1) Normalize the result, (2) Add or subtract the mantissas, (3) Align the mantissas, (4) Compare the exponents
 (a) 3, 4, 2, 1 (b) 4, 3, 2, 1
 (c) 2, 3, 4, 1 (d) 4, 2, 3, 1
- (x) Which of the following cache misses cannot be avoided by increasing the cache size?
 (a) Conflict Misses (b) Capacity Misses
 (c) Compulsory Misses (d) Read Misses

Fill in the blanks with the correct word

- (xi) The behavior of a pipeline can be illustrated with a _____ diagram.
- (xii) The _____ policy updates both the cache and the main memory simultaneously every time a write operation occurs.
- (xiii) The final addressing mode that we consider is _____.
- (xiv) Addressing modes like Auto-increment are particularly useful for traversing _____ structures in memory without needing extra instructions to update pointers.
- (xv) Zero-address instructions do not use explicit addresses because they operate on the top of a _____.

Group - B

2. (a) Draw the flowchart of the Restoring type of Division algorithm. Divide 15 by 3 with the help restoring type of division method. [[CO2](Apply/IOCQ)]
 (b) Differentiate between computer organization and computer architecture. Explain relative advantages and disadvantages between Direct Addressing Mode and Indirect Addressing Mode with example. [[CO1](Understand/LOCQ)]
(3 + 3) + (2 + 4) = 12
3. (a) Design a 4-bit serial adder and mark the delay in the circuit. Consider each gate incurs one gate delay. [[CO2](Apply/IOCQ)]
 (b) Design the Wallace tree adder to add 6 numbers. [[CO2](Apply/IOCQ)]
(3 + 4) + 5 = 12

Group - C

4. (a) Assume a memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time? [[CO3](Apply/IOCQ)]

- (b) In cache memory, if the address has 9 bits in the tag field and 12 bits in the index field, what will be the size of main memory and cache memory? *[[C03](Apply/IOCQ)]*
- (c) If the main memory is of 8K bytes and the cache memory is of 2K words and it uses associative mapping; then what will be the size of each word of cache memory? *[[C03](Apply/IOCQ)]*
- (d) Consider a memory system with a cache-access time of 100ns and a memory access time of 1200ns. If the effective access time is 20% greater than the cache access time, what is the hit ratio? *[[C03](Apply/IOCQ)]*
 $3 + 3 + 3 + 3 = 12$
5. (a) In a paging system, the logical address is 14-bits and the physical address is 12-bits. The page size is 512 bytes. If the Page Table currently maps Logical Page 2 to Physical Frame 5, what is the Physical Address corresponding to the Logical Address 1025? *[[C04](Apply/IOCQ)]*
- (b) A CPU produces 32-bit virtual addresses. The page size is 4 KB. The system has 512 MB of physical RAM. Calculate:
 i. The number of pages in the virtual address space.
 ii. The number of frames in physical memory.
 iii. The size of the Page Table (assume each Page Table Entry is 4 bytes). *[[C04](Apply/IOCQ)]*
 $6 + 6 = 12$

Group - D

6. Consider the Reservation Table given below:

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

- (i) Determine the set of Forbidden Latencies and Permissible Latencies, and the Initial Collision Vector.
- (ii) Draw the state diagram for scheduling this pipeline
- (iii) List all simple cycles. Especially point out the Greedy Cycles (GC).
- (iv) What is the Minimum Average Latency (MAL) of the pipeline? Specify lower and upper bounds of MAL?

[[C05] (Apply/IOCQ)]
 $(2 + 5 + 2 + 3) = 12$

7. (a) A non-pipelined processor has a cycle time of 100 ns. The same processor is redesigned with a 6-stage pipeline. Due to latch delays, the clock cycle of the pipelined version is 20 ns.
- i. Calculate the speedup of the pipeline for 1000 tasks.
- ii. Calculate the theoretical maximum speed-up.
- iii. Find the efficiency of the pipeline for 1000 tasks. *[[C05](Apply/IOCQ)]*

- (b) An instruction pipeline has 5 stages: IF, ID, EX, MEM, WB. The stage delays are 5ns, 4ns, 10ns, 8ns, and 5ns respectively. The interface registers have a delay of 1ns.
- Determine the clock cycle time.
 - Calculate the total time required to execute 200 instructions assuming no hazards.
 - If 20% of the instructions are conditional branches and the branch penalty is 3 cycles, calculate the effective CPI.
- [[CO5](Apply/HOCQ)]
- 6 + 6 = 12**

Group - E

8. (a) Differentiate between Data flow architecture and Control flow architecture.
[[CO6](Understand/LOCQ)]
- (b) Differentiate between Super-pipelining and Superscalar pipeline architecture.
[[CO6](Understand/LOCQ)]
- (c) How can hazards occur in executing the following set of instructions?
 I1: MOV R1, A ; [A] <- (R1)
 I2: ADD R2, R3; R3 <- (R3) + (R2)
 I3: SUB R4, R5; R5 <- (R4) - (R5)
 I4: NOP
 All the symbols have their usual meanings. You may assume a pipeline unit consisting of four stages.
 [[CO6](Analyse/HOCQ)]
3 + 3 + 6 = 12
9. (a) Consider a 5-stage pipeline (IF, ID, EX, MEM, WB). A program has a sequence of 10 instructions where 3 instructions are dependent on the immediate previous instruction's result. Calculate the total clock cycles required to complete the execution of this program without data forwarding (assuming stall) and with data forwarding.
[[CO6](Apply/IOCQ)]
- (b) Explain Data Hazards with a focus on RAW (Read After Write). Describe how Data Forwarding (Bypassing) acts as a counter-measure.
[[CO6](Understand/LOCQ)]
6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	18.75	68.75	12.50