DIGITAL ELECTRONICS
(AEI2201)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) If the number of bits in the sum exceeds the number of bits in each added numbers, it results
(a) Successor (b) Arithmetic Overflow
(c) Arithmetic Underflow (d) Predecessor

(ii) If one input of XOR gate connected to +5V, then it will be acting as a/an
(a) Inverter (b) Buffer
(c) Ex-Nor gate (d) None of the above

(iii) A priority encoder has four inputs I_0, I_1, I_2, and I_3 where I_3 has the highest priority and I_0 has the lowest priority. If $I_2 = 1$ and $I_1=1$, the output will be
(a) 00 (b) 01
(c) 10 (d) 11

(iv) The range of negative numbers for n-bit signed binary number system is
(a) -1 to $-(2^{n-1}-1)$ (b) 0 to -2^n-1
(c) -1 to -2^{n-1} (d) 0 to -2^n+1

(v) An A 3 bit adder circuit requires minimum
(a) two full adder and two half adder (b) three full adder
(c) two full adder and one half adder (d) one full adder and two half subtractor

(vi) The frequency of the output from a J-K flip flop, when J = 1, K = 1, and a clock with pulse waveform is given
(a) Twice the frequency of clock input
(b) Equal to the frequency of clock input
(c) Half the frequency of clock input
(d) Independent of the frequency of clock input

(vii) What input should be given to "R" when SR flip – flop is converted to JK flip – flop?
(a) K.Q' (b) J.Q
(c) J.Q' (d) K.Q

(viii) Which of the ADC circuit has the highest accuracy?
(a) Counter type (b) Dual slope Integrating type
(c) Flash type (d) Successive approximation type

(ix) In Programmable Array Logic (PAL)
(a) Both AND and OR arrays are programmable
(b) AND arrays are programmable OR arrays are fixed
(c) Both AND and OR arrays are fixed
(d) OR arrays are programmable AND arrays are fixed

(x) In a 4-bit digital to analog converter (DAC), reference voltage is 5V, then analog voltage corresponding to binary input 1001 is
(a) 4V (b) 3V (c) 1V (d) 2V

Fill in the blanks with the correct word

(xi) If $(1110212.20211)_3 = (X)_9$ then the value of X = _____ .

(xii) If the decimal number is a fraction then its binary equivalent is obtained by _____ the number continuously by 2.

(xiii) A frequency division of 2^N of the pulsed clock signal can be obtained by connecting _____ number of flip – flops asynchronously.

(xiv) The terminal count of a typical MOD-12 binary counter is _____.

(xv) The number of comparator circuits required to build a 3-bit Flash type ADC is _____.

Group - B

2. (a) Design the following logic gates NOT, AND, NOR, XOR using 2:1 Multiplexer? *[(CO2)(Apply/IOCQ)]*

(b) Perform $(- 4 - 5)_{10}$ using 4-bit signed binary operation and make a comment on the result. *[(CO1)(Understand/LOCQ)]*

6 + (4 + 2) = 12

3. (a) Minimize the given logic function in POS form
$Y = \sum m(0,2,5,7,12,14) + \sum d(4,6,8,10)$. *[(CO3)(Understand/LOCQ)]*

(b) Implement the following circuits:
(i) 3 input NOR gate using min no of 2 input NOR Gates
(ii) 3 input XNOR gate using min no of 2 input XNOR Gates. *[(CO2)(Understand/LOCQ)]*

6 + (3 + 3) = 12

Group - C

4. (a) Design a common circuit to perform both addition and subtraction of two 4-bit binary numbers. *[(CO3)(Apply/IOCQ)]*

(b) Implement the given logic function
$Y = \sum m(0,2,3,5,7,8,10,11,14,15,16,18,24,26,27,29,30,31)$ using 8:1 multiplexer. *[(CO3)(Understand/LOCQ)]*

6 + 6 = 12

5. (a) Design a 4-bit odd parity generator circuit. *[(CO3)(Apply/IOCQ)]*
   (b) Design a 4-bit Full adder circuit using carry look-ahead adder logic. *[(CO3)(Understand/LOCQ)]*

6 + 6 = 12

Group - D

6. (a) What is the racing problem in J-K flip flop? Explain the remedy for this problem with necessary circuit and output wave forms. *[(CO4)(Understand/LOCQ)]*
   (b) Design an asynchronous counter to count from 0 to 9. *[(CO4)(Understand/LOCQ)]*

(2 + 5) + 5 = 12

7. (a) Design an asynchronous counter to start the count at 2 and stop the count at 8 and start the count again from 2. *[(CO4)(Apply/IOCQ)]*
   (b) Design and analyze a frequency divider circuit whose output frequency, f_0 is divided by 16 of the clock frequency. *[(CO4)(Understand/LOCQ)]*

7 + 5 = 12

Group - E

8. (a) Design a NOR gate using CMOS logic. *[(CO6)(Understand/LOCQ)]*
   (b) Consider an 8-bit binary-weighted resistors DAC with reference voltage, V_R = 5 V and R_f = R. (i) What is the maximum output voltage (in magnitude)? (ii) Find the output voltage corresponding to the input 1010 1101. *[(CO5)(Apply/IOCQ)]*

4 + (4 + 4) = 12

9. (a) Write a short note on R-2R Ladder type DAC. *[(CO5)(Understand/LOCQ)]*
   (b) Implement the following logic functions by using PROM.
   $A=\sum m(1, 3, 5, 7)$, $B=\sum m(0, 2, 4, 7, 8, 10)$, $C=\sum m(1, 3, 9, 11, 12, 14)$ *[(CO5)(Apply/IOCQ)]*

4 + 8 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	57.3	42.7	0