PROCESSOR FUNDAMENTALS AND MICROCONTROLLERS
(ECE3103)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) What is the function of the HL pair in memory interfacing?
(a) Arithmetic operations (b) Temporary data storage
(c) Address pointer (d) Stack pointer

(ii) Which of the following is true about RISC architecture?
(a) Micro coded control unit (b) Fewer instructions with fixed length
(c) Uses CISC processors (d) Complex instructions with multiple cycles

(iii) The instruction OUT cannot send data from any register other than
(a) Program Counter (b) Register B
(c) Accumulator (d) Flag register

(iv) In ARM architecture, the instruction set that offers 16-bit compressed instructions is.
(a) ARM 32 (b) Thumb (c) Cortex (d) Neon

(v) Numeric data processor (floating point unit) is integrated with
(a) 8085 (b) 80486 (c) 8086 (d) 80386

(vi) Intel's MMX (MultiMedia eXtensions) technology was introduced in
(a) i286 (b) i386 (c) i486 (d) Pentium

(vii) When the 8255A is operating in Mode 0, what type of data transfer is supported?
(a) Simple input or output (b) Strobed input or output
(c) Handshaking input/output (d) Bi-directional data transfer

(viii) Which command word is used to initialize the 8259A during system setup?
(a) Initialization Command Word (ICW) (b) Operation Command Word (OCW)
(c) Mode Set Command Word (MSCW) (d) Control Command Word (CCW)

(ix) The internal RAM memory of the 8051 is
(a) 32 bytes (b) 64 bytes
(c) 128 bytes (d) None of these

(x) Register used to hold the address of the next instruction to be executed in 8051 is

(a) Data Pointer (DPTR) (b) Program Counter (PC)
(c) Stack Pointer (SP) (d) Accumulator (A)

Fill in the blanks with the correct word

(xi) Instruction MVI A, 05H is an example of _____ addressing.

(xii) The 80386 processor supports a _____bit address bus, allowing access to 4 GB

(xiii) The ARM instruction set that allows both 32-bit and 16-bit execution is called _____.

(xiv) The CPU responds to the DMA controller's HOLD request by sending the _____ signal, indicating that it has relinquished control of the bus.

(xv) The ___ addressing mode is used for instructions like MOV A, #25H, where the data is specified as part of the instruction.

Group - B

2. (a) Draw and label the block diagram of 8085. *[(CO1)(Remember/LOCQ]*
   (b) Mention the role of each of the following registers: PC, SP, Accumulator, and Flag Register. *[(CO1)(Understand/LOCQ)]*
   (c) Write an 8085 ALP to load the 16 bits number 2050H in the register pair HL involving LXI and MVI codes. Differentiate between two instructions. *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

3. (a) Explain how stack works in 8085 using PUSH and POP. *[(CO2)(Understand/LOCQ)]*
   (b) Evaluate the importance of RIM and SIM in interrupt management. *[(CO2)(Apply/IOCQ)]*
   (c) Differentiate between the instructions RRC & RAR with proper diagrams. *[(CO2)(Analyze/IOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Compare the features of 80386 & 80486. *[(CO3)(Analyze/IOCQ)]*
   (b) How can 80486 execute 15.0 MIPS at 25 MHz? *[(CO3)(Understand/LOCQ)]*
   (c) What is unaligned memory access? How is this problem addressed in i486? *[(CO3)(Apply/IOCQ)]*

4 + 4 + (2 + 2) = 12

5. (a) Write an 8086 ALP to transfer a block of 5 bytes from memory starting at 4101H to a destination starting at 5108H using MOVSB and REP *[(CO3)(Apply/IOCQ)]*
   (b) Explain the difference between the MUL and IMUL instructions in 8086 and mention how overflow is handled in both cases. *[(CO3)(Analyze/IOCQ)]*

(c) Explain with an example how a physical address can be generated from a segment address in 8086. *[(CO3)(Analyze/IOCQ)]*

6 + 4 +2 = 12

Group - D

6. (a) Draw the architecture of the 8255A with proper labelling of each block. *[(CO4)(Remember/LOCQ)]*

(b) Identify the functions of the Interrupt Request Register (IRR), In-Service Register (ISR), and Interrupt Mask Register (IMR) of 8259 PIC. *[(CO4)(Understand/LOCQ)]*

(c) How does the READY signal ensure safe timing between the 8237A and slower I/O or memory devices? *[(CO4)(Analyse/IOCQ)]*

4 + 6 + 2 = 12

7. (a) Calculate the count and write the control word of 8254 to generate a 1 KHz square wave from Counter 1 if the input clock is 2 MHz. *[(CO4)(Apply/IOCQ)]*

(b) Differentiate between Slave Mode and Master Mode of 8237A operation with respect to control flow and CPU involvement. *[(CO4)(Analyse/IOCQ)]*

(c) Why is the Priority Resolver essential in 8259A? *[(CO4)(Understand/LOCQ)]*

4 + 6 + 2 = 12

Group - E

8. (a) Describe the role of the Stack Pointer and Program Status Word (PSW) during subroutine calls and arithmetic operations. *[(CO5)(Understand/IOCQ]*

(b) Which mode of 8051 timer is useful in periodic timing applications & explain how? *[(CO5)(Understand/LOCQ)]*

(c) Identify the addressing mode of the following instructions of 8051 microcontroller:-

(i) MOV A, #0F5H (ii) ADD R6, A (iii) MOV DPTR, #5660H
(iv) MOVR4, 7FH (v) MOV A, @R0 (vi) MOVC A, @A+DPTR

[(CO5)(Apply/IOCQ)]

4 + 2 + 6 = 12

9. (a) Write 8051 ALP to copy the value 55H into RAM locations 40H to 44H using:
(i) Direct addressing
(ii) Indirect addressing with loop instruction. *[(CO6)(Apply/IOCQ)]*

(b) Write the 8051 ALP to generate a 5 ms pulse width on pin P2.3 of 8051. Assume a crystal frequency of 11.0592 MHz. (given that $(60928)_{10} = (EE00)_H$). *[(CO6)(Create/HOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	31.25	62.5	6.25