B.TECH/IT/3RD SEM/INFO 2102/2016

COMPUTER ORGANIZATION
(INFO 2102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Cache memory is made upon
(a) bipolar Semiconductor
(b) unipolar semi conductor device
(c) optical disk
(d) magnetic storage.

(ii) The Principle of locality justifies the use of
(a) interrupt (b) polling
(c) DMA (d) cache memory.

(iii) "Flops" and "MIPS" are related to the term speed of
(a) processor (b) primary memory
(c) both (a) & (b) (d) none of these.

(iv) MOV B, A is
(a) immediate addressing (b) register addressing
(c) direct addressing (d) indirect addressing mode.

(v) When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero?
(a) 1's complement (b) 2's complement
(c) both (a) and (b) (d) none of the above.

(vi) Virtual memory system allows the employment of
(a) more than address space (b) more than hard disk capacity
(c) External address (d) none.

(vii) The value of biased exponent in IEEE754 single precession format is
(a) 127 (b) 254 (c) 128 (d) 256.

(viii) How many address bits are required for 1024 ×8 memory chip?
(a) 1024 (b) 5 (c) 10 (d) 12.

(ix) "Delayed Branching" is related to
(a) pipeline hazard (b) pipeline remedy
(c) both (a) & (b) (d) none of these.

(x) DVD writer is a _____ access memory.
(a) semi random (b) serial
(c) random (d) non- serial.

Group – B

2. (a) What is addressing mode? Briefly explain Class-I type of addressing mode.

(b) What is Von-Neuman bottle-neck? What is the solution of this problem?

(2 + 4) + (4 + 2) = 12

3. (a) Assume the instruction set I={x, y, z, p, q}. The probability of occurrences of the instructions are 40%, 30%, 10%, 15%, 5% respectively. Design the instruction codes using Huffman coding.

(b) Compare RISC format and CISC format.

(c) Critically comment "Hoffman Coding" is done in CISC architecture.

(d) Suppose we have a 64 bit machine and 64 bit Operating systems, then what will be the size of memory buffer register (MBR) or at most how many bits it can transfer synchronously.

3 + 3 + 3 + 3 = 12

Group – C

4. (a) Draw a "ripple carry" adder circuit and a "carry Look Ahead" Adder circuit.

(b) What is the time complexity for propagating carry in "ripple carry" adder?

(c) Show one occurrence where the time complexity of Booth Algorithm as same as the Sequential Multiplication method.

(d) Apply Booth algorithm to multiply +14 and –12.

4 + 1 + 2 + 5 = 12

5. (a) Define IEEE (32bit) floating point format. Why is Biased exponent required?

   (b) Represent $(120.75)_{10}$ to IEEE 32 format.

   (c) Draw 8 bit adder subtractor circuit and explain the logic clearly.

(3 + 1) + 4 + 4 = 12

Group – D

6. (a) Suppose two levels of hierarchy memory M_1 and M_2, where the memory access times are 10^{-9} sec and 10^{-6} sec respectively. Hit ratio of top-level memory is 60%. Calculate average access time.

   (b) Design 1 bit RAM using basic gates.

   (c) Design 16 × 4-memory chips using 4 × 2-memory chips.

   (d) Assume requested pages are 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7. Number of memory slots are four. Apply LRU page replacement policy and sketch each instance of placement.

3 + 2 + 3 + 4 = 12

7. (a) "Set Associative Mapping is combination of Associative Mapping and Direct Mapping Technique" — justify.

   (b) Show the BUS connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip 512 × 8 bit size. Assume the CPU has 8 bit data bus and 16 bit address bus. Clearly specify generation of chip select signals.

6 + 6 = 12

Group – E

8. (a) Draw the I/O organization of Computer with simple I/O devices.

   (b) What is "Bus arbitration"? Draw different types of arbitration.

   (c) Differentiate between the concept of Memory mapped I/O and I/O mapped I/O.

4 + 4 + 4 = 12

9. (a) Derive the speed up formula of Pipeline. When the maximum speed up is achieved? What is cycle stealing?

   (b) Define pipeline hazard. Draw a pipelined execution diagram for the following code segment.
   ADD r1, r2, r3

SUB r4, r5, r6
MUL r8, r9, r10
DIV r12, r13, r14
Consider the pipeline as five stage.

(2 + 2 + 2) + (2 + 4) = 12