ADVANCED NANO DEVICES
(VLSI 5242)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Hot electron effect causes
(a) Oxide wear out and breakdown (b) Change in threshold voltage
(c) Finite gate current (d) All of the above.

(ii) The condition for punch-through is
(a) electrons are generated by impact ionization
(b) device operates in breakdown region
(c) drain and source depletion regions touch each other
(d) channel length is less than mean free path between collision of charge carriers.

(iii) Use of High-k material as the gate dielectric of a MOSFET leads to a _____mobility.
(a) lower (b) higher (c) unaltered (d) very high.

(iv) Which of the following mechanisms is responsible for DIBL (Drain Induced Barrier Lowering)?
(a) Electric field penetration into the channel
(b) Source/drain resistance increase
(c) Gate tunneling current
(d) Impact ionization.

(v) The threshold voltage of a MOSFET decreases if:
(a) The oxide thickness is reduced (b) The channel doping is increased
(c) The gate work function is changed (d) A high-K material is used.

(vi) Source and drain in nMOS device are isolated by _____
(a) a single diode (b) two diodes
(c) three diodes (d) four diodes.

(vii) Which of the following helps in reducing leakage current in MOSFETs?
(a) Decreasing oxide thickness (b) Using underlap design
(c) Increasing channel doping (d) Both (b) and (c).

(viii) The effective channel length of a MOSFET in saturation decreases with increase in
(a) Gate voltage (b) Drain voltage
(c) Source voltage (d) Body voltage.

(ix) Sub threshold conduction takes place predominantly by
(a) drift (b) diffusion
(c) both drift and diffusion (d) tunnelling.

(x) The cut off frequency, f_T , of the MOSFET is
(a) proportional to transconductance(g_m) and inversely proportionalto total capacitance between gate to source/drain (C_{gs}+ C_{gd})
(b) proportional to transconductance (g_m) and total capacitancebetween gate to source/drain (C_{gs}+ C_{gd})
(c) inversely proportional to transconductance (g_m) and totalcapacitance between gate to source/drain (C_{gs}+ C_{gd})
(d) inversely proportional to transconductance(gm) and totalcapacitance between gate to source/drain (C_{gs}+ C_{gd}).

Fill in the blanks with the correct word

(xi) DIBL (Drain-Induced Barrier Lowering) leads to a reduction in the device's _____ as the drain voltage increases.

(xii) High-K gate dielectric _____ the gate threshold voltage.

(xiii) The mobility degradation in nanoscale MOSFETs is primarily due to _____ scattering.

(xiv) Gate-induced drain leakage (GIDL) occurs due to _____ tunneling in the depletion region near the drain junction.

(xv) SiGe heterojunctions are used in CMOS technology to improve _____ by enhancing carrier transport properties.

Group - B

2. (a) State the limitations of the SiO_2 scaling. Explain how these may be overcome by the use of a high-K material as the gate dielectric. *[(CO2)(Analyze/IOCQ)]*
(b) List the basic requirements of a high-K oxide. State some limitations of using high-K oxides. *[(CO2)(Remember/LOCQ)]*

(2 + 4) + (3 + 3) = 12

3. (a) Briefly discuss the velocity overshoot effect in a scaled MOSFET. *[(CO1)(Analyze/IOCQ)]*
(b) To determine the inversion carrier mobility from experimental results, consider an n channel MOSFET having channel width 15 μm, channel length 2 μm and C_{ox} =6.9 × 10^{-8} F/cm^2.Assume that the drain current in the non saturation region for V_{DS} =0.1V is I_D=35μA at V_{GS} =1.5V and I_D=75μA at V_{GS} =2.5V. *[CO1/ Evaluate /IOCQ]*

5 + 7 = 12

Group - C

4. (a) Draw the cross-sectional diagram of a planar DG-MOSFET and compare its performance to that of an SOI device. *[CO4/ Remember/LOCQ]*
   (b) How does substrate doping influence SCEs in MOSFETs? Why is the substrate chosen to be undoped in scaled DG-MOSFETs? *[CO1/Analyse/IOCQ]*

6 + 6 = 12

5. (a) Explain with suitable expression, how the Effective Oxide Thickness (EOT) improves the gate leakage currents. *[CO2/Analyse/IOCQ]*
   (b) What are the limitations of Effective Oxide Thickness and how it can be improved? *[CO2/Understand/LOCQ]*
   (c) List the advantages offered by an FDSOI MOSFET. *[CO3/ Remember/LOCQ]*

5 + 4 + 3 = 12

Group - D

6. (a) What is parasitic capacitance? What are sources of parasitic capacitances in the MOSFET? *[CO1/Understand/LOCQ]*
   (b) Draw the small signal equivalent circuit of a MOSFET and show the parasitic capacitances in it. *[CO1/Create/HOCQ]*

(2 + 4) + 6 = 12

7. (a) Explain why FinFETs have better immunity to the Short Channel Effects? *[CO4/Analyse/IOCQ]*
   (b) Describe with the help of necessary illustration why ON resistance increases in the Double Gate underlap MOSFET structure. *[CO4/Analyse/IOCQ]*
   (c) Explain how ON current (Ion) is improved and DIBL is suppressed in the Double Gate Underlap MOSFET structure. *[CO4/Analyse/IOCQ]*

4 + 4 + 4 = 12

Group - E

8. (a) Explain the band alignment and carrier transport mechanisms in Si/SiGe heterostructures. *[CO5/ Analyse/IOCQ]*
   (b) How does strain engineering in SiGe heterojunctions improve carrier mobility? *[CO5/ Analyse/IOCQ]*

6 + 6 = 12

9. (a) Explain with suitable band diagrams the different possible structures when a narrow band gap and a wide band gap material form a heterojunction. *[CO5/Analyse/IOCQ]*
   (b) Explain the impact of different types of traps and bulk traps on the performance of HEMTs. How the interface influence threshold voltage stability? *[CO5/Analyse/IOCQ]*

6 + (4 + 2) = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	26.04	67.71	6.25