ADVANCED VLSI PROCESSOR
(VLSI 5241)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) A common bus system is designed for 16 registers 32 bits each using muxes. How many mux are needed and what is the size of each?
(a) 32, 16 to 1 (b) 16, 32 to 1
(c) 8, 16 to 1 (d) 16, 8 to 1

(ii) The Microinstructions are stored in
(a) Control memory (b) Cache memory
(c) Main memory (d) Flash Memory

(iii) A VLIW architecture places _____ instructions in a _____ word
(a) Multiple, Single (b) Single, Single
(c) Single, Multiple (d) Multiple, Multiple

(iv) The size of ALU in TMS320 DSP family is
(a) 32 bit (b) 16 bit
(c) 8 bit (d) 64 bit

(v) For ARM 7 the number of OS modes are
(a) 5 (b) 6
(c) 7 (d) 8

(vi) In ARM Registers R15 serves as the _____
(a) Program Counter (b) Link Register
(c) Stack Pointer (d) Program Status Register

(vii) Limitation of a uniprocessors leading to CMP
(a) Limited instruction and data parallelism
(b) Increase in clock speed limited by heat dissipation
(c) With increase in number of transistors the microprocessor design and debugging cost and complexity increases
(d) All of the above

(viii) The number of switches required to inter-connect between N input devices to N output device is of order

(a) N*N (b) Ln(N)
(c) N (d) N*N

(ix) In shared memory system _____ the time for memory access depends on location of data

(a) FLASH (b) NUMA
(c) USB (d) UMA

(x) Architecture that has the ability to issue simultaneously four operations is

(a) SISD (b) VLIW
(c) CISC (d) RISC

Fill in the blanks with the correct word

(xi) The number of 128x8 memory chips needed to provide a memory capacity of 4096x16 is _____

(xii) Harvard Architecture uses _____ memory bus and storage for Program and Data.

(xiii) To accommodate a 64-word stack, the minimum Stack Pointer (SP) size should be of _____ bits.

(xiv) In parallel computing _____ grained means data is communicated infrequently, after large amounts of computation.

(xv) In distributed memory topology the data exchange between processors are done by _____ passing.

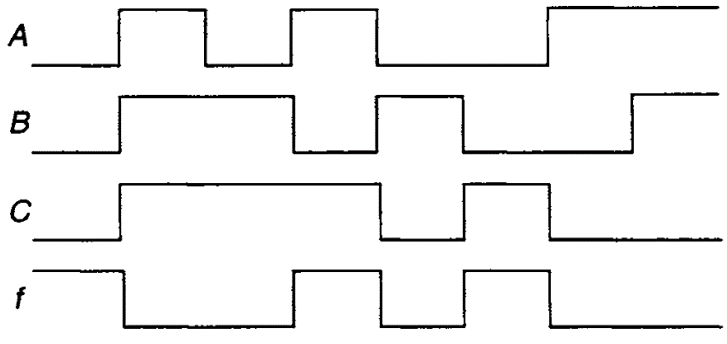
Group - B

2. (a) Design the control unit for the following register transfer statements using two 4 bit registers R1 and R2 and a 4 bit adder.

xT: R1 ← R1 + R2
x'T: R1 ← R2. *[(CO1)(Analyze/IOCQ)]*

(b) What are the main differences between Von Neumann architecture and Harvard architecture? What is a Von Neumann bottleneck? *[(CO1)(Remember/LOCQ)]*

(c) Given the timing diagram shown in the figure below find the displayed function f expressed as a sum of minterms and also find the function as a product of maxterms. Next simplify the minterm expression, using the Boolean theorems, and find the inverse of the simplified expression.



[(CO1)(Analyze/LOCQ)]

4 + 4 + 4 = 12

3. (a) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word in memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64registers, and an address part. (i) How many bits are there in the operation code, register code part, and the address part. (ii) Draw the instruction word format and indicate the number of bits in each part. (iii) How many inputs are there in the data and the address inputs of the memory? *[(CO1)(Analyse/LOCQ)]*

(b) What is the difference between a direct and an indirect addressing mode instruction? How many references to memory are needed for each type of instruction to bring an operand to a processor register? Illustrate with example. *[(CO1)(Remember/LOCQ)]*

(c) A nonpipelined system takes 50 ns to process a task. The same task can be processed in 6 segment pipeline with a clock cycle of 10 ns. Determine the speed ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? *[(CO1)(Apply/LOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Is VLIW architecture just limited to DSP processor? If not, have there been any new VLIW chip released for other workloads. What is the difference between VLIW & EPIC? *[(CO3)(Remember /LOCQ)]*

(b) In TMS320C5X, let the content AR0 be 2345h and the content of data memory location 1500h be 6789h, before executing the instruction SMMR AR0, #1500h. After executing the instruction, what will be contents of AR0 and data memory location? *[(CO3)(Apply/IOCQ)]*

(c) Explain how convolution is performed using a single MAC unit. *[(CO3)(Remember /HOCQ)]*

4 + 4 + 4 = 12

5. (a) Design a floating-point adder pipeline to add 100 floating point numbers. *[(CO1)(Analyze/LOCQ)]*

(b) Briefly define the following terms: (i) True dependency, (ii) Resource Conflicts, (iii) Anti dependency. *[(CO1)(Understand/IOCQ)]*

(c) Consider the following assembly language program:

I1: Move R3, R7 /R3 ← (R7)/
I2: Load R8, (R3) /R8 ← Memory (R3)/
I3: Add R3, R3, 4 /R3 ← (R3) + 4/
I4: Load R9, (R3) /R9 ← Memory (R3)/
I5: BLE R8, R9, L3 /Branch if (R9) > (R8)/

This program includes WAW, RAW, and WAR dependencies. Show these *[(CO1)(Apply/IOCQ)]*

4 + 3 + 5 = 12

Group - D

6. (a) What is an hardware accelerator? Explain with examples and mention its uses. *[(CO4)(Apply/IOCQ)]*

(b) What is size of Registers if ARM7? How many registers are used in the USER mode? How program status is handled in ARM instructions? *[(CO5)(Understand/LOCQ)]*

(c) State functions of ARM registers R13, R14, R15, and CPSR. *[(CO5)(Remember/LOCQ)]*

4 + (1 + 1 + 2) + 4 = 12

7. (a) Explain the concept of virtual memory. What is a page table? Explain how a page table links a page in virtual memory to physical memory? *[(CO5)(Remember/LOCQ)]*

(b) What is demand paging? What is a page fault? Describe page replacement policies (any two). What is page thrashing? Discuss the effect of page size on this scheme? *[(CO5)(Remember/LOCQ)]*

(c) Describe what is "locality of reference" and how "cache performance" can be measured quantitatively. *[(CO5)(Remember/LOCQ)]*

3 + 5 + 4 = 12

Group - E

8. (a) List the benefits of processor customization using SOC (System on Chip) design. *[(CO6)(Understand/LOCQ)]*

(b) When a design use FPGA over PSoC and vice versa? *[(CO6)(Understand/LOCQ)]*

(c) Let a be the percentage of program code that can be executed simultaneously by n processors in a computer system. Assume that the remaining code must be executed sequentially by a single processor. Each processor has an execution rate of x MIPS, (i) Derive an expression for the effective MIPS rate when using the system for exclusive execution of this program in terms of n, a, and x. (ii) If n = 16, and x = 4 MIPS, determine the value of a that will yield a system performance of 40 MIPS. *[(CO5)(Apply/IOCQ)]*

4 + 2 + 6 = 12

9. (a) What are the limitations of an uniprocessor? *[(CO5)(Understand/LOCQ)]*

(b) How does a CMP (Chip Multiprocessor) resolve this issues? *[(CO5)(Understand/LOCQ)]*

(c) A weather forecasting computation requires 250 billion floating point operations. The problem is processed in a super computer that can perform 100 mega flops *[(CO5)(Apply/IOCQ)]*

4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	65.62	30.21	4.17