# LOW POWER VLSI DESIGN
## (VLSI 5232)

**Time Allotted : 2½ hrs** **Full Marks : 60**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A

1. Answer any twelve: **12 × 1 = 12**

*Choose the correct alternative for the following*

(i) Dynamic Power Changes with $C_L$ in below way
(a) Decreases with increase in $C_L$
(b) Increases with increase in $C_L$
(c) Does not Change with $C_L$
(d) Initially Increases and then Decreases with increase in $C_L$

(ii) For a 2 Input AND Gate, if Signal Probability of Input A is 1/3 and Signal Probability of Input B is 1/4, then Signal Probability of AND Gate Output is
(a) 1/3 (b) 1/4 (c) 1/12 (d) 11/12

(iii) If Threshold Voltage of NMOS and PMOS is reduced by 10%, then Dynamic Energy Dissipation of the Inverter will Change by
(a) 10% (b) 20% (c) 5% (d) will not Change

(iv) FINFET Transistor Technology Started from Below Process Node in Industry
(a) 14nm (b) 45nm (c) 32nm (d) 22nm

(v) For a 2 Input NAND Gate, Leakage Current is Minimum when Input A and B are as follows:
(a) A=0, B=0 (b) A=0, B=1 (c) A=1, B=0 (d) A=1, B=1

(vi) For a CMOS Inverter, when Input is Logic 1, Below is True
(a) NMOS will have Channel Leakage
(b) PMOS will have Channel Leakage
(c) Both NMOS and PMOS will have Channel Leakage
(d) None of NMOS and PMOS will have Channel Leakage

(vii) If $C_L$ Load Capacitance is Increased, then Dynamic Power dissipation of CMOS Inverter
(a) Increases (b) Decreases
(c) Initially Increases and then Decreases (d) Remains Same

(viii) If Input Rise and Fall Time is Increased, then Short Circuit Current of CMOS Inverter
(a) Increases (b) Decreases
(c) Initially Increases and then Decreases (d) Remains Same

(ix) For Large SRAM Memory Array below Comment is Correct
(a) Read Dynamic Power is More than Write Dynamic Power
(b) Read Dynamic Power is Less than Write Dynamic Power
(c) Read Dynamic Power is same as Write Dynamic Power
(d) Read Dynamic Power is negligible and can be ignored

(x) Power Reduction Opportunity is Maximum if Worst Setup Margin in Chip is
(a) -10ps (b) 0ps (c) +10ps (d) +100ps

*Fill in the blanks with the correct word*

(xi) GIDL stands for _____.

(xii) For a NMOS Transistor, Channel Leakage is _____ than Gate Leakage.

(xiii) If Activity Factor Decreases, then Dynamic Power _____

(xiv) If $C_L$ Increases, then Short Circuit Power _____

(xv) $I_{ON}/I_{OFF}$ of FINFET is _____ than Planer Transistor

## Group - B

2. (a) Explain Glitch Power with Example. *[(CO1)(Analyse/IOCQ)]*
(b) What are the sources of Switching Capacitance ($C_L$) connected at the Output of a Digital Gate? *[(CO1)(Remember/LOCQ)]*

**6 + 6 = 12**

3. (a) Explain DVS with Example. *[(CO2)(Analyse/IOCQ)]*
(b) Derive Activity Factor of 2 Input XOR Gate Output if Signal Probability of Input A is 1/3 and Signal Probability of Input B is 2/3 *[(CO1)(Evaluate/HOCQ)]*

**6 + 6 = 12**

## Group - C

4. (a) To Reduce Gate Leakage what Technique was adopted in Advanced Process Nodes ? Explain the Technique. *[(CO3)(Analyse/IOCQ)]*
(b) Explain how $I_{ON}/I_{OFF}$ Current can be increased in FINFET Structure. *[(CO3)(Analyse/IOCQ)]*

**6 + 6 = 12**

5. (a) Explain how Device Down Sizing Technique can help reducing Chip Leakage Power and Still Meeting Frequency Target of the Chip. *[(CO3)(Analyse/IOCQ)]*
(b) Explain different Power Supply Gating Techniques to reduce Chip Leakage Power *[(CO3)(Analyse/IOCQ)]*

**6 + 6 = 12**

## Group - D

6. (a) Derive Activity Factor of 2 Input NAND Gate Output if Signal Probability of Input A is $P_A$ and Signal Probability of Input B is $P_B$. *[(CO1)(Analyse/IOCQ)]*

   (b) Explain Miller Effect on $C_{GD}$ Component of Parasitic Capacitance. *[(CO1)(Analyse/IOCQ)]*

**6 + 6 = 12**

7. (a) Plot PDP (Power Delay Product) (Y Axis) vs Gate Sizing (X Axis) Curve for a Digital Gate, say CMOS Inverter and explain the nature of the Curve. *[(CO1)(Analyse/IOCQ)]*

   (b) Plot Delay (Y Axis) vs Threshold Voltage (X Axis) Curve for a Digital Gate, say CMOS Inverter for different Supply Voltage ($V_{DD}$) and explain the nature of the Curve. *[(CO1)(Analyse/IOCQ)]*

**6 + 6 = 12**

## Group - E

8. (a) How 1-Transistor DRAM Array is less Leaky than 4 Transistor DRAM Array, Explain with Diagram. *[(CO5)(Analyse/IOCQ)]*

   (b) Why Pre-charge Voltage for 1 Transistor DRAM is used as $V_{dd}/2$ instead of $V_{dd}$? *[(CO5)(Analyse/IOCQ)]*

**6 + 6 = 12**

9. (a) Which Memory consumes higher Dynamic Power, "128 Entries x 2K Bits" or "2K Entries x 128 Bits? Give Justification. Consider both as SRAM Memory. *[(CO5)(Evaluate/HOCQ)]*

   (b) Explain how ROM Programming (Mask ROM) can save Leakage Power. *[(CO5)(Analyse/IOCQ)]*

**6 + 6 = 12**

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| Cognition Level | LOCQ | IOCQ | HOCQ |
|---|---|---|---|
| Percentage distribution | 6.23 | 81.25 | 12.5 |