# VLSI DESIGN, TESTING AND VERIFICATION
## (VLSI 5202)

**Time Allotted : 2½ hrs** **Full Marks : 60**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A

1. Answer any twelve: **12 × 1 = 12**

*Choose the correct alternative for the following*

(i) Memory which needs Dynamic Refresh is
(a) Flash (b) Latch (c) SRAM (d) DRAM

(ii) For a 6 Address Bits and 8 Data I/O Bits SRAM Memory, Number of SRAM Bit-Cells are
(a) 256 (b) 512 (c) 1024 (d) 128

(iii) Putting More VIAs in a Contact Helps to
(a) Reduce Contact Capacitance (b) Reduce Contact Resistance
(c) Increase Contact Capacitance (d) Increases Contact Resistance

(iv) In Nano Technology, Most Popular Interconnect Material is
(a) Gold (b) Silver (c) Copper (d) Platinum

(v) In a Flip-Flop Based System, $T_{cq}$ of Generating Flop is 20ps, $T_{setup}$ of Sampling Flop is 30ps, $T_{logic}$ of Combinational Logic Cone is 150ps for worst Timing Path. Maximum Frequency the System can operate is (ignore Clock Skew)
(a) 10 GHz (b) 8 GHz (c) 5 GHz (d) 2 GHz

(vi) A Timing Path In a Flip-Flop Based System has Hold Margin of +20ps. If Cycle time of Clock is Decreased by 20ps, then New Hold Margin will be
(a) +40ps (b) +20ps (c) 0ps (d) -20ps

(vii) Function Y = ABC + D can be implemented by using CMOS Logic having Minimum Number of Transistor as
(a) 8 (b) 10 (c) 12 (d) 14

(viii) A 4 Input NAND Gate has $W_n$ = 4um for Each NMOS, the $W_{neff}$ value is
(a) 4um (b) 2um (c) 1um (d) 16um

(ix) D-Algorithm is Directly Related to
(a) DFT (b) Scan (c) ATPG (d) BIST

(x) Input Test Vector to find Stuck-at-0 at output of 2 Input AND Gate is
(a) 00 (b) 01 (c) 10 (d) 11

*Fill in the blanks with the correct word*

(xi) ATPG Stands for _____.

(xii) DPM Stands for _____.

(xiii) The Transistor used in Flash Memory Bit-Cell is Called _____.

(xiv) Full Form of STA is _____.

(xv) With Increase of Threshold Voltage of NMOS and PMOS, Delay of CMOS Inverter _____.

## Group - B

2. (a) For a Memory of 1024 Entries and 64 Bits, what is best possible Folding scheme? How Many Row Address, How Many Column Address and what is Column Mixing Scheme? *[(CO1)(Evaluate/HOCQ)]*

(b) Draw 6 Transistor SRAM Cell with Interface Signals. *[(CO1)(Understand/LOCQ)]*

**8 + 4 = 12**

3. (a) Implement 7 to 128 Decoder using Optimized Number of Logic Gates. *[(CO1)(Evaluate/HOCQ)]*

(b) Explain Programmed NOR Based Mask ROM Operation with Circuit Diagram. *[(CO1)(Analyse/IOCQ)]*

**6 + 6 = 12**

## Group - C

4. (a) Explain Different Components of Interconnect Capacitance with Diagram *[(CO2)(Understand/LOCQ)]*

(b) Prove that wire RC Delay is Proportional to Square of the Length of the Wire. *[(CO2)(Evaluate/HOCQ)]*

**6 + 6 = 12**

5. (a) 1mm Wire with 400mohms/um and 0.2fF/um has to be Modelled using 3 PI Segments. What will be Individual Resistance and Capacitance Component, explain with Circuit Diagram. *[(CO2)(Evaluate/HOCQ)]*

(b) Using Elmore Delay Model, prove that Wire Delay Can be Reduced maximum way if Driver Side Resistance and Receiver Side Capacitance is Reduced. *[(CO2)(Evaluate/HOCQ)]*

**6 + 6 = 12**

## Group - D

6. (a) Explain with Waveform D → Q Timing Path and CLK → Q Timing Path for a Level 1 D-Latch. *[(CO3)(Analyse/IOCQ)]*

(b) For a Flipflop Based System, $T_{CQ}$ of Generating Flop = 30ps, $T_{LOGIC}$ of Combinational Circuit = 250ps, $T_{SETUP}$ of Sampling Flop = 20ps, $T_{HOLD}$ of Sampling Flop = 60ps. $T_{CYCLE}$ of CLK = 400ps. Clock Skew = 40ps. What is Setup Margin for the Timing Path? *[(CO4)(Evaluate/HOCQ)]*

**6 + 6 = 12**

7. (a) Explain How Timing Characterization of Digital Gate is Performed? *[(CO3)(Analyse/IOCQ)]*

(b) Draw Circuit of 2 to 1 Mux using Transmission Gate. *[(CO3)(Understand/LOCQ)]*

(c) Explain H-Tree Clock Network with Circuit Diagram. *[(CO5)(Analyse/IOCQ)]*

**4 + 4 + 4 = 12**

## Group - E

8. (a) What is the Test Vector to Detect Stuck-at-0 at Output of 3 Input NOR Gate? *[(CO6)(Evaluate/HOCQ)]*

(b) Consider a 2 Input CMOS NOR Gate with A, B as Inputs and Y as Output. What is the Test Vector to Detect whether there is Stuck-Short in the NMOS Connected to A Input? *[(CO6)(Evaluate/HOCQ)]*

**6 + 6 = 12**

9. (a) Why Post Silicon Debug is Needed? *[(CO6)(Understand/LOCQ)]*

(b) What are Sources of Process Variation? *[(CO6)(Understand/LOCQ)]*

(c) Explain Transistor Stuck-Open Fault with an Example. *[(CO6)(Analyse/IOCQ)]*

**4 + 4 + 4 = 12**

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| Cognition Level | LOCQ | IOCQ | HOCQ |
|---|---|---|---|
| Percentage distribution | 22.9 | 25 | 52.1 |