ANALOG VLSI IC DESIGN
(VLSI 5201)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Linear amplification can be obtained from common-source MOSFET amplifier when biased in
(a) Saturation region (b) Linear region
(c) Subthrehold region (d) only exactly at $V_{DS} = V_{DS(sat)}$

(ii) Practical current mirror circuits deviate from ideal behaviour due to
(a) Channel-length modulation effect (b) Threshold voltage offset between two transistors
(c) Imperfect geometrical matching (d) All of the above

(iii) The substrate of the NMOS transistor is connected to
(a) Most negative supply in the system (b) ground
(c) threshold voltage (d) most positive supply in the system

(iv) Multiplication in the time domain corresponds to
(a) Multiplication in the frequency domain (b) Convolution in the frequency domain
(c) Addition in the frequency domain (d) Division in the frequency domain

(v) For a good design of MOSFET, the relationship between the thermal noise arising from the gate resistance and the channel should satisfy
(a) $4kT\frac{R_G}{3} << \frac{4kT\gamma}{g_m}$ (b) $4kT\frac{R_G}{3} >> \frac{4kT\gamma}{g_m}$
(c) $4kT\frac{R_G}{3} << 4kT\gamma g_m$ (d) $4kT\frac{R_G}{3} = \frac{4kT\gamma}{g_m}$

(vi) The error tolerance at the output of S/H (Sample / Hold) depends on the amplifier's
(a) Offset (b) Gain Error
(c) Linearity (d) All of the above

(vii) A *4-bit R-2R* digital-to-analog converter has a reference of *5volts*. What is the analog output for the input code *0101*
(a) 0.3125V (b) 3.125V
(c) 0.78125V (d) -3.125V

(viii) Considering VREF = 1V, as the digital word increases by 1 bit, the output of the ideal 3-bit DAC should jump by
(a) 0.25V (b) 0.0625V
(c) 0.33V (d) 0.125V

(ix) The frequency of the signal applied to the switched-capacitor circuit should satisfy the the criteria
(a) $f_{signal} << f_{clock}$ (b) $f_{signal} >> f_{clock}$
(c) $f_{signal} = 2f_{clock}$ (d) $f_{clock} = 2f_{signal}$

(x) The number of inverter stages in a ring oscillator is given by
(a) 1 (b) 2
(c) 3 (d) Anyone of (a), (b), (c)

Fill in the blanks with the correct word

(xi) An ideal differential amplifier should have common-mode voltage gain _____.

(xii) A good current mirror should have _____ (high / low) output resistance.

(xiii) Integral Nonlinearity (INL) is one important _____ (static / dynamic) characteristics of the DAC.

(xiv) The full form of PLL is _____.

(xv) Switched capacitors accumulate the _____ noise of the switches.

Group - B

2. (a) Briefly explain the voltage transfer characteristics of a basic resistive load differential amplifier circuit. *[(CO2)(Understand/LOCQ)]*
   (b) Deduce the ICMR of this type of circuit. *[(CO2)(Analyze/IOCQ)]*
   (c) Consider the circuit in Fig. 1 in which M2 is twice as wide as M1. Calculate the small-signal gain if the bias values of V_{in1} and V_{in2} are equal. *[(CO2)(Evaluate/HOCQ)]*

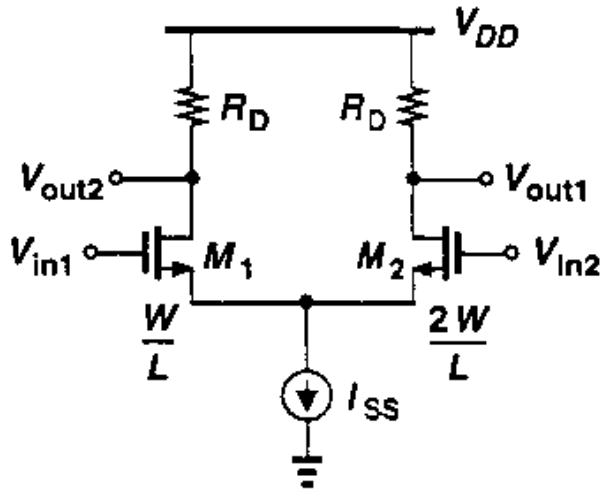

Fig. 1

4 + 5 + 3 = 12

3. (a) Briefly explain the current –voltage characteristics of a current sink and source. *[(CO1)(Apply/IOCQ)]*
   (b) Derive the small-signal voltage gain of a push-pull amplifier from its small-signal equivalent circuit. *[(CO2)(Analyze/IOCQ)]*
   (c) Consider a discrete common-source MOSFET amplifier shown in Fig. 2. Determine its small-signal voltage gain, its input resistance and the largest allowable input signal. The transistor has $V_{th} = 1.5V$, $k_n'(W/L) = 0.25mA/V^2$, and $V_A = 50V$. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest. *[(CO1)(Evaluate/HOCQ)]*

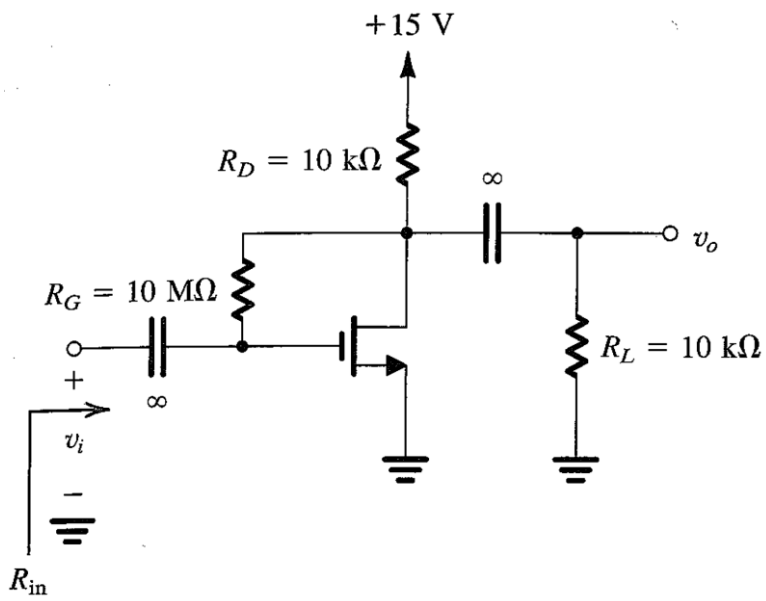

Fig. 2

4 + 5 + 3 = 12

Group - C

4. (a) Briefly discuss the effects of nonlinearity in RF circuits. *[(CO3)(Understand/LOCQ)]*
   (b) An analog multiplier mixes its two inputs $x_1(t)$ and $x_2(t)$, ideally producing an output $y(t) = kx_1(t)x_2(t)$, where k is a constant. Assume, $x_1(t) = A_1Cos\omega_1 t$ and $x_2(t)=A_2Cos\omega_2(t)$. (i) If the mixer is ideal, determine the frequency components, (ii) If the input port sensing $x_2(t)$ suffers from third-order nonlinearity, determine the output frequency components. *[(CO3)(Apply/LOCQ)]*
   (c) In most circuits, one terminal of the inductor(s) is at *ac* ground. Which terminal of the structure should be grounded in Fig. 3. *[(CO3)(Apply/LOCQ)]*

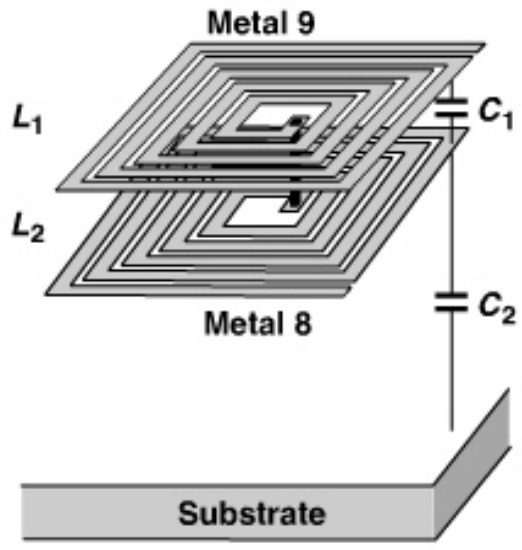

Fig. 3

4 + 5 + 3 = 12

5. (a) Briefly explain the phenomenon of cross-modulation. *[(CO3)(Understand/LOCQ)]*

(b) Suppose an interferer contains phase modulation but not amplitude modulation. Does cross modulation occur in this case? Justify. *[(CO3)(Apply/IOCQ)]*

(c) A Low-Noise amplifier senses a *-80dBm* signal at *2.410GHz* and two *-20dBm* interferers at *2.420GHz* and *2.430GHz*. What IIP_3 is required if the InterModulation (IM) must remain *20dB* below the signal? For simplicity, assume 50Ω interfaces at the input and output. *[(CO3)(Evaluate/HOCQ)]*

4 + 3 + 5 = 12

Group - D

6. (a) Explain the *INL* and *DNL* of a digital-to-analog converter graphically. *[(CO4)(Understand/LOCQ)]*

(b) Determine the *DNL* for the *3-bit* nonideal DAC whose transfer curve is shown in the Fig. 4. Assume that $V_{REF} = 5V$. *[(CO4)(Apply/IOCQ)]*

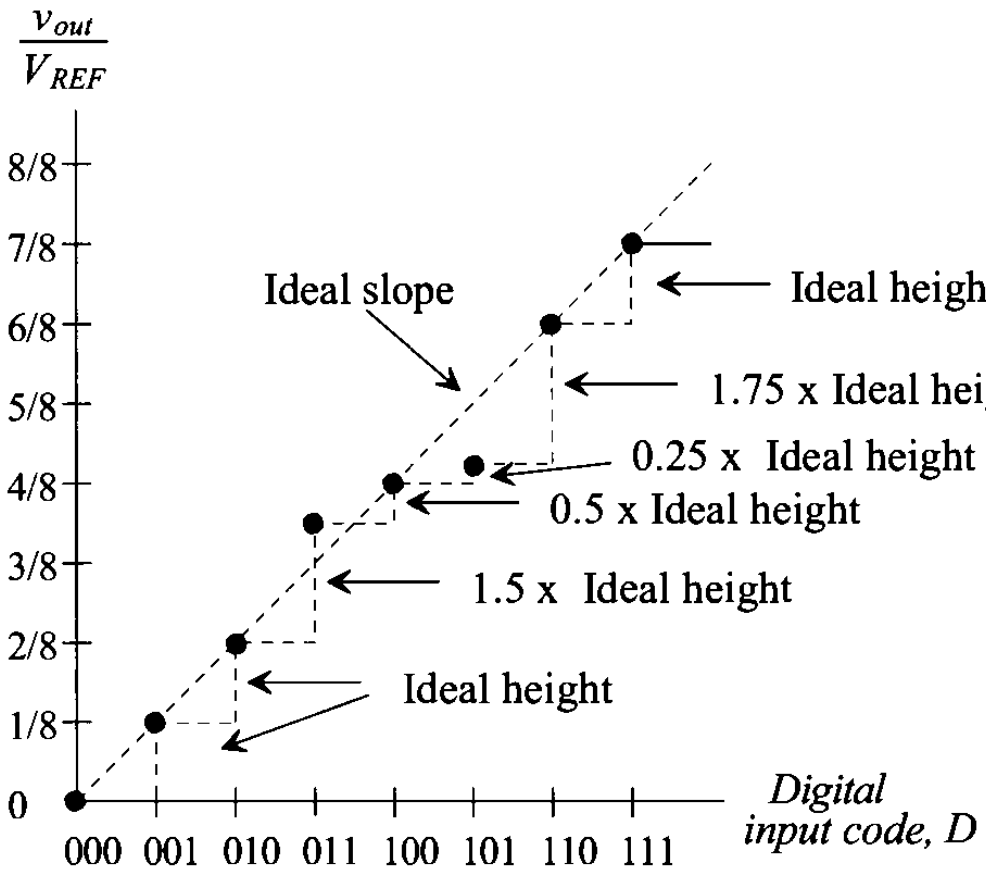

Fig. 4

(c) Draw the *DNL* curve for the *3-bit* nonideal *DAC*. *[(CO4)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

7. (a) Determine the resolution for a *DAC* if the output voltage is desired to change in *1mV* increments while using a reference voltage of *5V*. *[(CO4)(Apply/IOCQ)]*

(b) Determine the *INL* for the *ADC* whose transfer curve is illustrated in Fig. 5. Assume that $V_{REF} = 5V$. *[(CO4)(Apply/IOCQ)]*

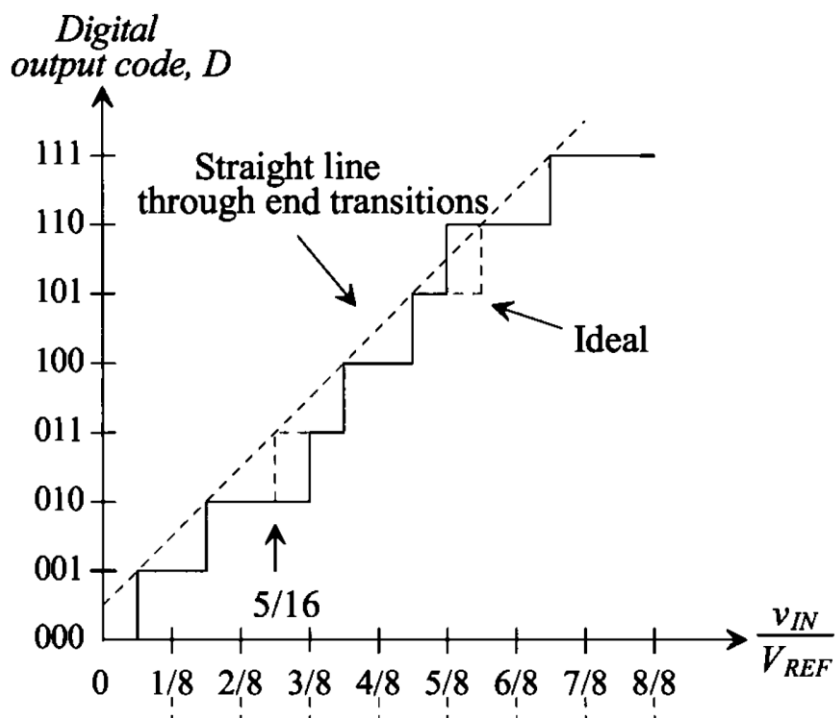

Fig. 5

(c) Draw the Quantization error (Q_e) in units of *LSBs*. *[(CO4)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Mention the advantages of the switched-capacitor circuits. *[(CO5)(Understand/LOCQ)]*

(b) Emulate the resistor equivalent of the parallel switched capacitor circuit. *[(CO5)(Apply/IOCQ)]*

(c) Design a parallel switched capacitor circuit which will emulate 1MΩ resistor and the clock frequency is 100KHz. Determine the value of capacitance. *[(CO5)(Apply/LOCQ)]*

4 + 5 + 3 = 12

9. (a) Explain the Barkhausen criteria for oscillation. *[(CO6)(Understand/LOCQ)]*

(b) Analyze the stability of two-pole amplifier system with proper graphical illustration. *[(CO6)(Analyze/IOCQ)]*

(c) Determine the minimum voltage required voltage gain per stage in the four-stage oscillator shown in Fig. 6. How many signal phases are provided by the circuit? *[(CO6)(Evaluate/HOCQ)]*

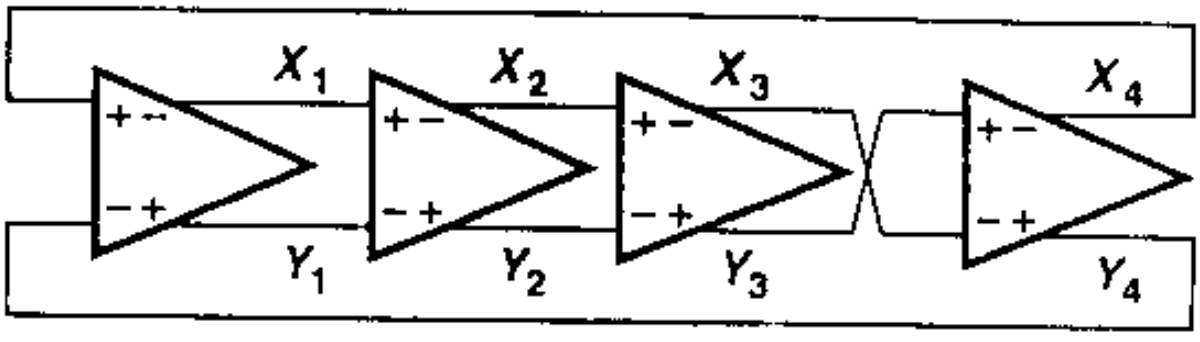

Fig. 6

4 + 3 + 5 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	36.46	38.54	25