EMBEDDED SYSTEMS DESIGN
(VLSI 5102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Which one of the following is not a contributing parameter for Time-to-market an embedded system?
(a) Design time (b) Manufacturing time
(c) Testing time (d) Maintainability time.

(ii) What is the primary advantage of using a microcontroller over a general-purpose processor in embedded systems?
(a) Higher processing power (b) Lower cost and power consumption
(c) Greater flexibility (d) Better multitasking capabilities.

(iii) System which is strictly not embedded is a
(a) Digital Camera (b) Treadmills
(c) Vending machine (d) Personal Laptop.

(iv) What is the primary function of a watchdog timer in an embedded system?
(a) To measure time intervals
(b) To generate precise time delays
(c) To monitor the system for faults and reset it if necessary
(d) To control real-time tasks.

(v) What is the primary function of a UART?
(a) To convert parallel data to serial data (b) To amplify digital signals
(c) To filter analog signals (d) To generate clock signals.

(vi) The 8051 microcontroller has a word size of
(a) 64 bit (b) 32 bit (c) 8 bit (d) 16 bit

(vii) Which special function register (SFR) is used to control the serial port mode of operation?
(a) SCON (b) TMOD (c) TCON (d) PCON.

(viii) How many separate address and data lines are needed for a RAM with a size of 16K × 8?

(a) 10 addresses, 16 data lines (b) 14 addresses, 8 data lines
(c) 12 addresses, 16 data lines (d) 12 addresses, 12 data lines.

(ix) DMA can be used to transfer data directly between memory and a

(a) Peripheral unit (b) Flip-flop
(c) Counter (d) Register

(x) Which 8051 port is commonly used for interfacing a 16x2 LCD?

(a) Port 0 (b) Port 1 (c) Port 2 (d) Port 3.

Fill in the blanks with the correct word

(xi) In ideal Top-Down design process the next step after behavioural specification is _____ specification.

(xii) Verilog and _____ are two popular Hardware Description Languages (HDLs) used for RTL design.

(xiii) _____ design describes components and their interconnections using hardware description language.

(xiv) The first segment of the internal RAM of 8051 microcontroller is divided into _____ register banks.

(xv) The fastest analog-to digital converter (ADC) is _____ type ADC.

Group - B

2. (a) Which are the common characteristics of an embedded system? *[(CO1)(Understand/LOCQ)]*

(b) Describe about the time-to-market design metric for an embedded system and derive an expression for percentage revenue loss in terms of delay. *[(CO1)(Analyze/IOCQ)]*

(c) Explain the NRE and unit cost design metrics with proper examples. *[(CO1)(Understand/LOCQ)]*

4 + 4 + 4 = 12

3. (a) Which are the differences between a real time and non-real time systems? *[(CO1)(Analyse/IOCQ)]*

(b) Explain why single purpose processors are more preferred over general purpose processors in case of embedded system design. *[(CO1)(Understand/LOCQ)]*

(c) What is the role of RTOS in embedded system? *[(CO1) (Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) What are the key components of an FSM? *[(CO2)(Remember/LOCQ)]*

(b) How do you represent an FSM using a state diagram and a state table? *[(CO2)(Apply/IOCQ)]*

(c) Illustrate the basic steps to design of a custom Single Purpose Processor. *[(CO2) (Understand /LOCQ)]*

4 + 4 + 4 = 12

5. (a) What is Harvard Architecture? Explain briefly using a block diagram. *[(CO2)(Remember/LOCQ)]*

(b) State the major differences between superscalar and VLIW processor architectures. *[(CO2)(Analyse/IOCQ)]*

(c) A 4 stage pipeline system takes 20ns to process a sub operation in each stage. The pipeline executes 100 tasks in sequence. What is the speed up ratio? *[(CO2)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Analyze the serial data transmission modes with 8051 microcontroller. *[(CO3)(Analyze/IOCQ)]*

(b) Add the unsigned numbers found in internal RAM locations 25H, 26H and 27H together and put the result in RAM locations 30H (MSB of Sum) and 31H (LSB of SUM). *[(CO3)(Apply/IOCQ)]*

8 + 4 = 12

7. (a) Explain briefly the ARM processor architecture with block schematic. *[(CO4)(Understand/LOCQ)]*

(b) The number A6h is placed somewhere in the external RAM between locations 0100h and 0200h. Write an assembly language program for 8051 microcontroller to find the address of that location and put that address in R6 (LSB) and R7 (MSB). *[(CO3)(Remember/LOCQ)]*

6 + 6 = 12

Group - E

8. (a) What are the key differences between SRAM and DRAM in terms of speed, cost, and volatility? *[(CO5)(Analyze/IOCQ)]*

(b) How does the internal structure of SRAM and DRAM cells differ? *[(CO5)(Analyze/IOCQ)]*

(c) Design an 8 × 4 size EPROM using floating Gate MOSFETs as programmable switches. *[(CO5)(Create/HOCQ)]*

4 + 4 + 4 = 12

9. (a) What is the difference between isolated I/O and memory mapped I/O? *[(CO5)(Understand/LOCQ)]*

(b) Explain DMA data transfer between memory and terminal peripheral. *[(CO6)(Understand/LOCQ)]*

(c) Why DMA based I/O is better than other I/O based technique? *[(CO6)(Analyze/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	45.83	50	4.17