DIGITAL VLSI IC DESIGN
(VLSI 5101)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Minimum Number of Transistors in CMOS Logic Y = ABC + DE is
(a) 8 (b) 10 (c) 12 (d) 14

(ii) The threshold voltage of an ideal inverter is
(a) V_{DD} (b) $V_{DD}/2$ (c) $V_{DD}/4$ (d) $V_{DD}/3$

(iii) Minimum number of transistors to design a 2- input NAND gate using CMOS Logic is
(a) 2 (b) 4 (c) 6 (d) 8.

(iv) As per Moore's Law Number of Transistors per Die/Chip gets Doubled every
(a) 6 Months (b) 12 Months
(c) 18 Months (d) 24 Months

(v) Memory Design is normally done using below Design Approach
(a) FPGA (b) Gate Array
(c) Full Custom Design (d) Standard Cell Based Semi Custom Design

(vi) SRAM based FPGA is
(a) One Time Programmable (b) Read Only
(c) Reprogrammable (d) None of the above.

(vii) In VHDL code, "entity" section tells:
(a) Behavioural description (b) Data flow description
(c) I/O Declaration (d) Structural description

(viii) To implement 31 States in State diagram of a FSM, Number of Flip-flops needed are
(a) 5 (b) 4 (c) 3 (d) 2

(ix) KL Algorithm is used for
(a) Floorplan (b) Placement
(c) Routing (d) Partitioning

(x) BDD is used in
(a) Partitioning (b) High Level Synthesis
(c) Logic Level Synthesis (d) Floorplan.

Fill in the blanks with the correct word

(xi) GSI Stands For _____.

(xii) Full Form of PLA is _____.

(xiii) The Euler path traverses each edge (branch) of the graph exactly _____.

(xiv) The full form of ASIC is _____.

(xv) Dynamic Gate followed by Static Gate Pair is Called _____.

Group - B

2. (a) Implement 2 input XOR Gate using Transmission Gate Logic. *[(CO1)(Analyse/IOCQ)]*
(b) Implement Positive D-Latch (Level-1) using Transmission Gate Based Circuit. *[(CO1)(Analyse/IOCQ)]*
(c) Implement Negative Edge Triggered Flip-Flop using Positive D-Latch and any Digital CMOS Combinational Logic Gate. *[(CO1)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

3. (a) Why Dynamic Gate Output cannot be connected as Input to Next Stage Dynamic Gate? *[(CO1)(Understand/LOCQ)]*
(b) Find Logical Effort of 3 Input CMOS NOR Gate. *[(CO1)(Evaluate/HOCQ)]*
(c) Explain Charge Sharing Noise in Dynamic Circuit. *[(CO1)(Understand/LOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Explain the differences between Full Custom Design and Standard Cell based Semi Custom Design. *[(CO3)(Analyse/IOCQ)]*
(b) Implement Y = ABC + AC + BC using PLA. *[(CO3)(Evaluate/HOCQ)]*

6 + 6 = 12

5. (a) Describe Different Components of FPGA. *[(CO3)(Remember/LOCQ)]*
(b) Implement Y = A+B using 2 Input LUT. *[(CO3)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - D

6. (a) Draw Data Flow Graph and Construct the scheduling of all the operations in the function *f=(a+b+c+d)*e* with two adders and a multiplier within three control steps. *[(CO5)(Evaluate/HOCQ)]*

(b) Write VHDL Code for Rising Edge Triggered D-Flip Flop Gate using Behavioural Model. *[(CO4)(Analyse/IOCQ)]*

6 + 6 = 12

7. (a) Design the data flow graph (DFG) and provide the scheduling solution for the operation:
*e = 12x + (x*x) + (y*y*y)*
having the highest possible speed of design where maximum *2* multiplication (*) allowed per cycle of clock. *[(CO5)(Evaluate/HOCQ)]*

(b) Write VHDL Code for 2 input AND Gate using Dataflow Model. *[(CO4)(Analyse/LOCQ)]*

8 + 4 = 12

Group - E

8. (a) Draw flow diagram of Logic Synthesis. *[(CO5)(Remember/LOCQ)]*

(b) Implement BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a ≤ b ≤ c. *[(CO5)(Evaluate/HOCQ)]*

(c) Create ROBDD Diagram for the same function f and find out corresponding optimized Boolean Expression. *[(CO5)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

9. (a) For below Channel Routing Problem, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG):
Terminal Connection is as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection. Assume HV Layer (V = Metal 1, H = Metal 2).
[(CO6)(Evaluate/HOCQ)]

(b) Evaluate Optimum Channel Routing Solution for above case using Left Edge Algorithm. *[(CO6)(Evaluate/HOCQ)]*

8 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	22.92	20.83	56.25