MICROPROCESSORS AND MICROCONTROLLERS
(ECEN 3104)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) DAD H adds up the content of HL register pair to the content of
(a) HL register pair (b) BC register pair
(c) Accumulator (d) Stack pointer.

(ii) In an Intel 8085 Ready signal is used
(a) to indicate that the processor is ready for use
(b) to provide wait status when processor is communicating with slow peripheral devices
(c) to slow down a fast peripheral device
(d) none of these.

(iii) If the result of an arithmetic operation is zero then the flag which goes to set state is
(a) Sign (b) Zero (c) Carry (d) Parity.

(iv) LHLD 2080H is a 3-byte instruction with
(a) 5 Machine cycles and 16 T states
(b) 4 Machine cycles and 16 T states
(c) 5 Machine cycles and 15 T states
(d) 4 Machine cycles and 15 T states

(v) 8085 Pins IO/M(bar), S0, and S1 can be used to determine the
(a) Machine Cycle (b) Instruction Cycle
(c) T state (d) Program Cycle

(vi) During XRA instruction which of the following is true?
(a) Only S and Z flags are affected (b) Only S and P flags are affected
(c) S, Z and P flags are affected (d) All of them are true.

(vii) When the 8255A is operating in Mode 0, what type of data transfer is supported?
(a) Simple input or output (b) Strobe input or output
(c) Handshaking input/output (d) Bi-directional data transfer.

(viii) Which command word is used to initialize the 8259A during system setup?
(a) Initialization Command Word (ICW) (b) Operation Command Word (OCW)
(c) Mode Set Command Word (MSCW) (d) Control Command Word (CCW).

(ix) DPTR is a
(a) 8-bit register (b) 16-bit register
(c) 32-bit register (d) 12-bit register.

(x) Which register in the 8051 is used to hold the address of the next instruction to be executed?
(a) Data Pointer (DPTR) (b) Program Counter (PC)
(c) Stack Pointer (SP) (d) Accumulator (A).

Fill in the blanks with the correct word

(xi) MOV R, M is an example of _____ addressing mode.

(xii) The Fetch machine cycle of instruction "MOV A, B" has _____ T states.

(xiii) The CPU responds to the DMA controller's HOLD request by sending the _____ signal, indicating that it has relinquished control of the bus.

(xiv) The 8259A can handle up to _____ interrupt requests simultaneously.

(xv) In the 8051 microcontroller, the ___ addressing mode allows access to program memory using the PC (Program Counter) or DPTR.

Group - B

2. (a) Identify the instruction used for masking operation. Register A contains 8FH. State an instruction to remove the lower order 4 bits of register A through masking operation. Test the status of the Zero and Sign flag after the operation.
[(CO2)(Evaluate/HOCQ)]

(b) Define addressing modes. Identify different addressing modes in 8085 microprocessor. *[(CO2)(Understand/LOCQ)]*

(c) Classify different types of branch operations. Identify their functions in 8085.
[(CO2)(Understand/LOCQ)]

(d) Demonstrate the contents of all the registers and output at PORT1 if the following program is executed.

```
MVI B, 82H
MOV A, B
MOV C, A
MVI D, 37H
OUT PORT1
HALT.
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[(CO1, CO2)(Apply/IOCQ)]

3 + (1 + 2) + (2 + 2) + 2 = 12

3. (a) Identify the number of bytes in the following instructions:
(i) MOV A, B
(ii) MVI B, 56H
(iii) ADI 42H
(iv) DCX SP

(v) JNZ 6151H

(vi) CALL 2151H *[(CO2)(Understand/LOCQ)]*

(b) Use instructions to load the 16 bits number 2050H in the register pair HL involving LXI and MVI codes. Differentiate between two instructions. *[(CO2)(Apply/IOCQ)]*

(c) Differentiate with proper diagrams between the instructions RRC & RAR. *[(CO2)(Analyze/IOCQ)]*

3 + 4 + 5 = 12

Group - C

4. (a) Explain the operations of BIU and EU present in 8086 microprocessors. *[(CO4)(Understand/LOCQ)]*

(b) Explain the concept of maskable and non-maskable interrupts of 8085. *[(CO3)(Remember/LOCQ)]*

(c) Explain with an example how a physical address can be generated from a segment address in 8086. *[(CO4)(Understand/LOCQ)]*

3 + 6 + 3 = 12

5. (a) Design an interfacing circuit for a memory chip of size 256 x 8 such that the addresses will range from 0000H to 00FFH. Modify the hardware of the chip select line so that the address ranges from 8000 H to 80FF H. *[(CO3)(Design/HOCQ)]*

(b) The memory address of the last location of an 8K byte memory chip is FFFFH. Calculate the starting address. *[(CO3)(Apply/IOCQ)]*

(c) Compare between absolute and partial decoding with proper explanation *[(CO3)(Analyze/IOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Explain the functions of BSR mode and I/O mode of 8255A programmable peripheral interface. *[(CO5)(Understand/LOCQ)]*

(b) Explain the function of ICWs and OCWs of 8259A interrupt controller. *[(CO5)(Understand/LOCQ)]*

(c) Write instructions to generate a 1 kHz square wave from Counter 1. Assume the gate of Counter 1 is tied to +5V through a 10k resistor and port address for Counter 1 and control word register is 81H and 83H respectively. Explain the significance of connecting the gate to +5 V. *[(CO5)(Apply/IOCQ)]*

4 + 4 + 4 = 12

7. (a) Explain the various operating modes of the 8254 programmable interval timer. *[(CO5)(Understand/LOCQ)]*

(b) Explain the process of switching from slave mode to master mode in DMA. *[(CO5)(Understand/LOCQ)]*

(c) Design a BSR control word subroutine to set bits PC7 and PC3 and reset them after 10 ms. Assume that a delay subroutine is available and the Hex address of Port A = 80 H. *[(CO5)(Design/HOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Draw the flag register of 8051. *[(CO6)(Remember/LOCQ)]*

(b) Which one of the following is invalid instructions and explain the reasons for their invalidity.

(i) MOV R3, #804H
(ii) MOV R7, #f7H
(iii) MOV R7, R2
(iv) ADD R4, #32H *[(CO6)(Apply/IOCQ)]*

(c) Which register bank is default by nature? Explain clearly how one can switch register banks in 8051. *[(CO6)(Remember/LOCQ)]*

3 + 4 + (1 + 4) = 12

9. (a) Show the status of CY and P flags after the addition of 9CH and 64H in the following instructions. Also show the content of A.

MOV A, #9CH
ADD A, #64H *[(CO6)(Apply/IOCQ)]*

(b) Define register indirect addressing mode and indexed addressing mode. Give one example for each of them. *[(CO6)(Understand/LOCQ)]*

(c) Explain the steps required in enabling an interrupt in 8051. *[(CO6)(Understand/LOCQ)]*

4 + (2 + 2) + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	56.25	32.29	11.46