DIGITAL SYSTEMS DESIGN
(ECE2102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) The number of adjacent cells each cell can have in an n variable K-Map is
(a) n-1 (b) n (c) n+1 (d) 2n.

(ii) The code where all successive numbers differ from their preceding number by single bit is
(a) Alphanumeric Code (b) BCD
(c) Excess 3 (d) Gray.

(iii) A decoder with enable input can be used as
(a) Encoder (b) Parity Generator
(c) Multiplexer (d) Demultiplexer

(iv) A 4-variable logic expression can be realized by using only one
(a) 3-input NOR gate (b) 4:1 demultiplexer
(c) 16:1 multiplexer (d) none of these

(v) Which of the following circuit can be used as parallel to serial converter?
(a) Multiplexer (b) Demultiplexer
(c) Decoder (d) Digital counter.

(vi) What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?
(a) 0 to 2^n (b) 0 to $2^n + 1$
(c) 0 to $2^n - 1$ (d) 0 to $2^{n+1/2}$

(vii) Master-slave configuration is used in flip-flop to
(a) increase its clocking rate (b) reduce power dissipation
(c) eliminate race-around condition (d) improve its reliability

(viii) The number of flip-flops required for a mod-16 ring counter is
(a) 4 (b) 8 (c) 15 (d) 16

(ix) The fastest ADC is
(a) counter-type (b) flash-type
(c) successive-approximation type (d) dual-slope type.

(x) Which family has the better noise margin?
(a) ECL (b) DTL (c) MOS (d) TTL.

Fill in the blanks with the correct word

(xi) A modulus-12 ring counter requires a minimum of _____.

(xii) Minimum number of 2-input NAND gates required to implement the function F = (X + Y) (Z + W) is _____.

(xiii) 1/4 as a binary number would be _____.

(xiv) The invalid range for an input to TTL logic is from _____.

(xv) The duty cycle of a square wave is _____.

Group - B

2. (a) Expand A' + B' to minterms and maxterms. *[(CO1)(Apply/IOCQ)]*
(b) Realize the following expression F=A *XOR* B *XOR* C using NAND logic. *[(CO1)(Apply/IOCQ)]*
(c) Add 41+44 in the 8421 BCD code. *[(CO1) (Apply/IOCQ)]*
(d) Convert the Gray code 1001 to its equivalent Binary code. *[(CO1)(Apply/IOCQ)]*

4 + 4 + 2 + 2 = 12

3. (a) Simplify the following function in SOP form using Quine MC-Cluskey method: $F(A, B, C, D)=\sum m(0,1,4,7,9,11,13,15) + \sum d(3,5)$ *[(CO1)(Evaluate/HOCQ)]*
(b) Subtract (-9) from (+12) in 2's complement system. *[(CO1)(Apply/IOCQ)]*

8 + 4 = 12

Group - C

4. (a) Implement the following function using 8:1 MUX: $F(A, B, C, D)=\sum m(1, 3, 4, 11, 12, 13, 14, 15)$. *[(CO3)(Evaluate/HOCQ)]*
(b) Design a Half-subtractor using only NAND gates. *[(CO2)(Apply/IOCQ)]*
(c) What is the difference between Decoder and Demultiplexer? *[(CO3)(Remember/LOCQ)]*

6 + 4 + 2 = 12

5. (a) Design a combinational circuit, which converts Excess-3 number to its corresponding BCD number. *[(CO3)(Evaluate/HOCQ)]*
(b) Design 1-bit magnitude comparator circuit using basic logic gates. *[(CO3)(Evaluate/HOCQ)]*
(c) Realize the following Boolean function using 3 to 8 line Decoder: $F(A, B, C)=\sum m(3,5,6,7)$. *[(CO3)(Evaluate/HOCQ)]*

4 + 4 + 4 = 12

Group - D

6. (a) Draw the gate level circuit diagram of a positive edge-triggered JK flip-flop and explain its operation with the help of a truth table. How is the race around condition eliminated? *[(CO4)(Remember/LOCQ)]*

   (b) What is a shift register? Distinguish between a shift register and a counter. *[(CO5)(Remember/LOCQ)]*

   (c) Design a 4-bit ring counter using J-K flip-flops. *[(CO5)(Create/HOCQ)]*

(4 + 2) + 3 + 3 = 12

7. (a) Draw a timing diagram of a 3-bit Twisted Ring counter. *[(CO5)(Remember/LOCQ)]*

   (b) Design a MOD-10 synchronous binary UP counter using J-K flip-flop and necessary logic gates. *[(CO5)(Create/HOCQ)]*

   (c) What is the lock-out condition of a counter? *[(CO5)(Remember/LOCQ)]*

3 + 7 + 2 = 12

Group - E

8. (a) Draw a dynamic RAM cell and explain its operation. *[(CO6)(Remember/LOCQ)]*

   (b) Explain the differences between PAL & PLA with a basic example. *[(CO6)(Apply/IOCQ)]*

   (c) Explain the operation of a programmable switch used in EEPROM. *[(CO6)(Apply/IOCQ)]*

4 + 4 + 4 = 12

9. (a) Explain the operation of CMOS inverter circuit with truth table. *[(CO6)(Analyse/HOCQ)]*

   (b) Design a 3-input NOR gate using CMOS logic family. *[(CO6)(Create/HOCQ)]*

   (c) State the differences static and dynamic RAMs. *[(CO6)(Remember/LOCQ)]*

4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	23.95	29.17	46.88