COMPUTER ORGANIZATION AND ARCHITECTURE
(INF2102)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) What is the default value of accumulator in booth's multiplication of two 4-bit binary numbers?
(a) 0 (b) 1 (c) 0000 (d) 00000.

(ii) The basic principle of Von-Neumann computer is _____.
(a) storing program and data in separate memory
(b) storing program and data in same memory
(c) using pipeline architecture
(d) none of these

(iii) The addressing mode/s, which uses the PC instead of a general purpose register is _____.
(a) Indexed with offset (b) Relative
(c) Direct (d) both Indexed with offset and direct

(iv) During the transfer of data between the processor and main memory we use _____.
(a) TLB (b) Buffers (c) Cache (d) none of the above

(v) For converting virtual address into physical address, the programs are divided into _____.
(a) Pages (b) Frames
(c) Segments (d) Blocks

(vi) Systolic array is an example of _____ architecture.
(a) MIMD (b) MISD (c) SIMD (d) SISD.

(vii) In super-scalar processors, _____ mode of execution is used.
(a) In-order (b) Post order (c) Out of order (d) None of the mentioned

(viii) Traditional multicomputers have been called as _____ machines.
(a) UMA (b) NORMA (c) COMA (d) NUMA

(ix) If the control signals are generated by combinational logic, then they are generated by a type of _____ controlled unit.
(a) Micro programmed (b) Software
(c) Logic (d) Hardwired

(x) _____ computer exploits spatial parallelism rather than temporal parallelism as in a pipelined computer
(a) SISD (b) SIMD (c) MISD (d) MIMD

Fill in the blanks with the correct word

(xi) When the processor executes multiple instructions at a time it is said to use _____.

(xii) The _____ plays a very vital role in case of super scalar processors.

(xiii) To increase the speed of memory access in pipelining, we make use of _____.

(xiv) If a system is 64 bit machine, then the length of each word will be _____ bytes.

(xv) There are two major classes of parallel computer, namely, _____ and _____.

Group - B

2. (a) Evaluate the multiplication of (-13) and (7) with the help of Booth Multiplication algorithm. *[(CO2)(Evaluate/HOCQ)]*

(b) X=(A*B)*(C/D)/E
Evaluate the above expression with the help of one address, two address and three address instructions. *[(CO2)(Evaluate/HOCQ)]*

6 + (2 × 3) = 12

3. Design a 1-bit ALU which will perform following operations
(i) Addition (ii) Subtraction (iii) AND (iv) OR (v) NOR (vi) NAND *[(CO2)(Analyse/HOCQ)]*

(6 × 2) = 12

Group - C

4. (a) Implement the bus connection with a CPU to connect four RAM chips of size 256 x 8 bits each and a ROM chip of size 256 x 8 bits. Assume the CPU has 8 bit data bus and 16 bit address bus. *[(CO3)(Analyse/HOCQ)]*

(b) Define write back and write through policies in cache memory. *[(CO4)(Remember/LOCQ)]*

(c) Explain different types of locality of references in memory system. *[(CO4)(Remember/LOCQ)]*

4 + 4 + 4 = 12

5. (a) (i) Determine how much faster a machine would run with a perfect cache that never missed.
Considering following assumption:
Instruction miss rate 5%.
Data miss rate 7%.
CPI is 3 (without any memory stalls).

Miss penalty 50 cycles.
32% of instructions are load/store.

(ii) Suppose that clock rate of the machine used in the previous example is doubled but the memory speed, cache misses, and miss rate are same. How much faster the machine be with the faster clock? *[(CO4)(Apply/IOCQ)]*

(b) Classify ROM(Read only Memory) in detail. *[(CO3)(Understand/LOCQ)]*

(4 + 4) + 4 = 12

Group - D

6. (a) Describe the asynchronous and synchronous model of linear pipeline processor with diagram. *[(CO5)(Remember/LOCQ)]*

(b) Consider the four-stage pipelined processor specified by the following reservation table.

	1	2	3	4	5	6	7
S1	X			X			X
S2		X			X		
S3			X			X	
S4				X	X		

(i) Determine the collision vector.
(ii) Draw the state transition diagram.
(iii) Find out the greedy cycle for each state.
(iv) Calculate MAL (Minimal Average Latency). *[(CO5)(Apply/IOCQ)]*

4 + (2 + 2 + 2 + 2) = 12

7. (a) A 400 MHz processor was used to execute a benchmark program with the following instruction mix and clock cycle counts.

Instruction type	Instruction count	Clock cycle count
Integer arithmetic	450000	1
Data transfer	320000	2
Floating point	150000	2
Control transfer	80000	2

Determine the effective CPI, MIPS rate and execution time for this program. *[(CO5)(Apply/IOCQ)]*

(b) Discuss the architecture of a vector supercomputer with diagram. *[(CO5)(Remember/LOCQ)]*

(2 + 2 + 2) + 6 = 12

Group - E

8. (a) Explain the Flynn's classification of computer architectures with block diagram. *[(CO6)(Understand/LOCQ)]*

(b) Discuss in detail the micro programmed control unit. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

9. (a) Describe the RISC and CISC computers with example. *[(CO6)(Remember/LOCQ)]*

(b) Explain the UMA, NUMA and COMA computers. *[(CO6)(Understand/LOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	47.91	22.91	29.16