DIGITAL CIRCUIT DESIGN
(ECE2002)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Which of the following is a self-complementing code?
(a) Excess-3 Code (b) Hamming Code
(c) Cyclic Code (d) Gray Code.

(ii) Simplified form of Boolean expression ($A+B' + A'B$) is
(a) 1 (b) 0 (c) C (d) C'

(iii) The octal equivalent of $(5EA)_{16}$ is
(a) 6543 (b) 2752 (c) 5722 (d) 3453

(iv) Add the two BCD numbers: 1001 + 0100 = ( )$_{BCD}$
(a) 10101111 (b) 01010000
(c) 00010011 (d) 00101011

(v) How many 3×8 decoders are required to construct a 4×16 decoder
(a) 2 (b) 3 (c) 4 (d) 8

(vi) In a general demultiplexer, there are ___ selector terminals, ___ input terminals and ____ output terminals
(a) 1,2n,3n (b) n,1,2^n
(c) n,2,n^3 (d) 4,2n,2^n

(vii) Maximum possible range of bit-count in an n-bit binary counter consisting of 'n' number of flip-flop is
(a) 0 to 2n (b) 0 to (2n+1)
(c) 0 to (2n-1) (d) 0 to (2n+1)/2

(viii) The race around condition in JK-FFs may be taken care of by
(a) Reducing the on time duration of the clock pulse width
(b) Using Master-Slave FFs
(c) Both (a) and (b)
(d) Connecting J and K inputs to 0

(ix) In the CMOS logic circuit realizing the 2 Input NOR the total number of transistors (PMOS and NMOS) required is
(a) 10 (b) 8 (c) 4 (d) 2

(x) The memory which is ultraviolet erasable and electrically programmable is
(a) RAM (b) EEPROM (c) PROM (d) EPROM.

Fill in the blanks with the correct word

(xi) Gray code of $(110101)_2$ is _____.

(xii) A decoder with 64 output lines has _____input lines.

(xiii) Number of FFs required for a MOD 12 ripple counter is _____.

(xiv) In a CMOS NOR gate, in the Pull Up, the 2 PMOS transistors are connected in _____ and in the Pull Down, the 2 NMOS are connected in _____.

(xv) _____ number of FFs are required to construct an 8 bit shift register.

Group - B

2. (a) Convert the following binary numbers into BCD
(i) $(100111.0101)_2$ (ii) $(0.101011)_2$. *[(CO1)(Apply/IOCQ)]*
(b) Realize Y=(A+C)(A+D')(A+B+C') using NOR gates only. *[(CO1)(Apply/IOCQ)]*
(c) Simplify the boolean expression (P'+R)(P'+R')(P'+Q+R'). *[(CO1)(Apply/IOCQ)]*

4 + 4 + 4 = 12

3. (a) Apply K-map method, to obtain minimal POS of $f(w,x,y,z)=m\sum(1,3,4,5,6,7,9,12,13)$ *[(CO1)(Analyse/IOCQ)]*
(b) Convert (i) $(743)_8 \rightarrow (\ )_{10}$ (ii) $(1100101)_{Gray} \rightarrow (\ )_2$ (iii) $(3421)_{10} \rightarrow (\ )_{EX\text{-}3}$ *[(CO1)(Remember/LOCQ)]*
(c) Write the decimal equivalent codes for the following canonical POS function
f(X,Y,Z)=(X+Y+Z')(X+Y'+Z')(X+Y+Z)(X'+Y+Z')(X'+Y'+Z') *[(CO1)(Analyze/IOCQ)]*

4 + (2 + 1 + 2) + 3 = 12

Group - C

4. (a) Show how a 8-input MUX is used to generate the function
Y=(ABC)'D +BCD+A(BC)'+ABC'D *[(CO3)(Evaluate/HOCQ)]*
(b) Implement a full adder circuit using decoder and OR gates. *[(CO2&CO3)(Apply/IOCQ)]*
(c) Design a four-bit binary parallel adder circuit using full-adder circuit blocks. *[(CO2)(Create/HOCQ)]*

4 + 4 + 4 = 12

5. (a) Design a single stage BCD adder. *[(CO2)(Analyse/IOCQ)]*
(b) Explain the advantages of a priority encoder over a standard encoder using truth tables of 4-line to 2-line standard encoder and a priority encoder. *[(CO3)(Understand/LOCQ)]*

(c) A 8 to 1 MUX is used to implement a function F(A,B,C,D). It has inputs A, B, C connected to selection lines S2, S1 and S0. The data inputs I0 to I7 are as follows. I0=I1=I5=D, I2=D', I6=I7=1, I3=I4=0. Determine the function F(A,B,C,D).

[(CO3)(Evaluate/HOCQ)]

4 + 3 + 5 = 12

Group - D

6. (a) Implement a clocked SR Flip flop with NOR gates and show its characteristic table. *[(CO4)(Understand/LOCQ)]*

(b) Design a MOD-8 ripple counter with T-FFs. *[(CO5)(Apply/IOCQ)]*

(c) Design a D latch with SR latch and explain with a function table how the indeterminate state is avoided. *[(CO4)(Apply/IOCQ)]*

4 + 4 + 4 = 12

7. (a) Convert T flip-flop to D flip flop. *[(CO4)(Apply/IOCQ)]*

(b) Explain the working principles of a Master Slave J - K flip flop. *[(CO4)(Understand/LOCQ)]*

(c) Design a Mod-4 synchronous up counter. *[(CO5)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - E

8. (a) Implement the function Y =A+B using CMOS logic circuit. *[(CO6)(Apply/IOCQ)]*

(b) Describe a CMOS inverter circuit and discuss its advantage over nMOS and Pmos circuits. *[(CO6)(Understand/LOCQ)]*

(c) Using CMOS gates construct a two input NAND gate and explain its working principle with a truth table. *[(CO6)(Apply/IOCQ)]*

4 + 4 + 4 = 12

9. (a) Explain the working principle of SERIAL-IN, PARALLEL-OUT shift register with suitable logic diagram. *[(CO5)(Understand/LOCQ)]*

(b) Differentiate between ROM and RAM. Explain the basic differences between EPROM and EEROM. *[(CO6)(Remember/LOCQ)]*

(c) Elaborate the functions of a PLD programmer. Explain the applications of PLA. *[(CO6)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	29.17	57.29	13.54