M.TECH/ECE(VLSI)/1ST SEM/VLSI 5131/2016

EMBEDDED SYSTEMS
(VLSI 5131)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) SOC means
(a) Multiple programs on chip
(b) a system distributed in different chips
(c) A partially filled system in a chip
(d) A single chip that would realize the entire system.

(ii) The number of active elements in a DRAM cell is
(a) 1 (b) 2 (c) 6 (d) 9.

(iii) DMA can be used to transfer data directly between memory and a
(a) peripheral unit (b) flipflop
(c) counter (d) register.

(iv) ARM Processors are designed to meet the needs of
(a) embedded real time systems (b) virtual memory
(c) cache (d) multi user.

(v) In Harvard Architecture, to access program and data memory
(a) same bus is used
(b) separate address bus and separate data bus is used
(c) separate address bus but same data bus is used
(d) same address bus but separate data bus is used.

(vi) The Logic family which takes the least power is
(a) TTL (b) ECL (c) RTL (d) CMOS.

(vii) The Logic family which is fastest is
(a) TTL (b) ECL (c) RTL (d) CMOS.

(viii) An embedded system must have
(a) hard disk (b) processor and memory
(c) operating system (d) processor and I/O units.

(ix) UART device
(a) receives parallel data and stores as parallel data
(b) receives serial data and stores as serial data
(c) receives serial data and stores as parallel data
(d) receives parallel data and stores as serial data.

(x) Which pin of port 3 has an alternative function as write control signal for external data memory?
(a) P3.8 (b) P3.3 (c) P3.6 (d) P3.1.

Group – B

2. (a) Classify Embedded System. Write down some application area of Embedded System. Give an example of an Embedded System with its block diagram.

(b) What do you mean by Design Metric? What are the design metrics to design an embedded system?

(2 + 2 + 4) + (1 + 3) = 12

3. (a) Explain Full Custom IC design, Semi Custom ASIC design, and design with PLD.

(b) Discuss their pros and cons. Use examples to show how a processor technology can be applied efficiently to a technique.

6 + 6 = 12

Group – C

4. (a) Compare General purpose, single purpose and application specific processor.

(b) What are the various operations present in RTL language? Represent the RTL statement, conditional statement and concurrent conditional statement for information transfer from one register to another. Do as directed: I. Obtain the circuit diagram from the RTL code if s=1 then R0←R1 else R0←R2. II. Obtain the RTL code for a 3-8 decoder.

4 + (2 + 4 + 2) = 12

5. (a) Sketch a communication diagram between CPU and the memory and I/O devices of a computer system, and briefly explain the function of interfacing unit between CPU and the devices.

   (b) Give the main reasons why DMA based I/O is better in some circumstances than interrupt driven I/O.

   (c) What is programmed I/O? Why is it not very useful compared to DMA?

   (d) Where does DMA mode of data transfer finds its use?

5 + 3 + 2 + 2 = 12

Group – D

6. (a) Discuss about the interrupts in the 8051 microcontroller. Describe the Timer Mode Control Register of 8051.

   (b) Write a program to generate 2 KHz square wave on pin P1.0 of port 1 of 8051 microcontroller using interrupt.

(5 + 3) + 4 =12

7. (a) Define the range of numbers possible in 8051 unsigned data.

   (b) List the timers of the 8051 and their associated registers.

   (c) Describe the two modes of the 8051 timers with examples.

2 + 4 + 6 = 12

Group – E

8. (a) Explain how a Keypad module can be interfaced with any embedded processor.

   (b) Describe the interfacing of a Flash type A/D Converter with an 8-bit processor.

6 + 6 = 12

9. (a) Explain the SRAM and DRAM. Compare their characteristics in terms of Reading and Writing.

   (b) What is cache mapping? Design a direct cache mapping scheme with main memory size of 16 Mbyte with word size of 16 bits. The Cache size is 16K lines. Each cache line can hold a main memory word plus the tag bits.

6 + 6 = 12