M.TECH/ECE(VLSI)/1ST SEM/VLSI 5102/2016

DIGITAL IC DESIGN
(VLSI 5102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Ideal Current Source has Resistance of value
(a) 0 ohm (b) Infinite
(c) 100 M ohm (d) 10 K ohm.

(ii) For a Standard Cell Layout
(a) height is fixed (b) width is fixed
(c) both height and width are fixed (d) none of above.

(iii) BDD is used in
(a) High Level Synthesis (b) Logic Synthesis
(c) Floorplan (d) Routing.

(iv) Minimum Number of Transistors in CMOS logic Y = AB + CD + EF is
(a) 10 (b) 12 (c) 14 (d) 8.

(v) LUT belongs to which of the following types of Circuits?
(a) Gate Array (b) CPLD (c) PLA (d) FPGA.

(vi) KL Algorithm is related to
(a) Routing (b) Partitioning
(c) Logic Synthesis (d) High Level Synthesis.

(vii) With decrease of V_{dd}, the Delay of an CMOS inverter
(a) increases (b) decreases
(c) remains same (d) becomes infinite.

(viii) The output of Physical Design is
(a) Logical Netlist (b) Circuit Diagram
(c) Layout (d) RTL.

(ix) 0.7 Technology Scaling enables Layout area scaling of
(a) 0.7 (b) 0.5 (c) 0.45 (d) 0.65.

(x) Stick Diagram represents _____of design.
(a) logic (b) circuit
(c) layout (d) architecture.

Group – B

2. (a) Draw Circuit Diagram of a D-Latch using CMOS Transmission Gate (TG).

(b) Draw Circuit Diagram of a Negative Edge Triggered D-Flip Flop using D-Latch.

(c) Draw Circuit Diagram of 2 input XOR gate using CMOS Logic.

(d) Draw Circuit Diagram of 2 input XOR gate using CMOS Transmission Gate (TG).

3 + 3 + 3 + 3 = 12

3. (a) What is the difference between "Micron based Design Rule" and "Lambda Based Design Rule"?

(b) What are the differences between Full Custom Design and Standard Cell based Semi Custom Design?

(c) Draw schematic of CMOS gate which represents function f = (A + BC + D).

(d) Draw Stick Diagram of the same CMOS circuit.

2 + 2 + 3 + 5 = 12

Group – C

4. (a) Draw Flow Diagram of Physical Layout Automation 3

(b) For Channel Routing Problem stated below, draw Horizontal Constraint Graph (HCG) and Vertical Constraint Graph (VCG)
Terminal Connection is as follows:
11122563040 ----- Upper Boundary
25055330604 ----- Lower Boundary
0 means no Connection.
Assume HV Layer (V = Metal 1, H = Metal 2)

(c) Provide Optimum Channel Routing Solution for above case using Left Edge Algorithm.

2 + 5 + 5 = 12

5. (a) Solve Euler Path Algorithm for the function f = C(A + B)'.

(b) Draw Stick Diagram accordingly.

(c) Describe the difference between Behavioural and Structural Model of VHDL coding using an example.

4 + 4 + 4 = 12

Group – D

6. (a) Draw flow diagram of High Level Synthesis.

(b) Draw flow diagram of Logic Synthesis.

(c) Draw BDD Diagram for function f = abc + ab'c + a'bc' + a'b'c' using Ordering of a $\leq$ b$\leq$ c.

(d) Create ROBDD Diagram and corresponding optimized Boolean expression.

3 + 3 + 3 + 3 = 12

7. Write short notes on
(i) FPGA.
(ii) Finite State Machine.
(iii) Technology Library Mapping for Logic Synthesis.

4 + 4 + 4 = 12

Group – E

8. (a) What are key limitations of pseudo-NMOS logic family?

(b) Why CMOS Transmission gate is used instead of NMOS pass transistor logic?

(c) Draw Circuit Diagram of a positive edge triggered D-Flip Flop.

(d) Draw Circuit Diagram of 16 input OR gate using Domino Circuit.

2 + 2 + 4 + 4 = 12

9. (a) Draw VTC Curve for CMOS Inverter and show various region.

(b) Draw Domino Implementation of 3 input NOR gate.

(c) Implement f = A.B Boolean logic using Transmission Gate.

3 + 4 + 5 = 12