M.TECH/ECE(VLSI)/1ST SEM/VLSI 5101/2016

VLSI DEVICE & MODELLING
(VLSI 5101)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) The MOSFET in its linear region of operation behaves like a
(a) resistor (b) capacitor (c) inductor (d) diode.

(ii) The Fermi levels of two systems in thermal equilibrium with no current flow through them must
(a) be equal (b) be unequal (c) disappear (d) split.

(iii) Most commonly used semiconductor material is
(a) Silicon (b) Germanium
(c) Mixture of silicon and germanium (d) None of the above.

(iv) Doping in semiconductor
(a) will decrease scattering (b) will increase scattering
(c) will increase the speed of the device (d) none of these.

(v) In a MOSFET channel with strong inversion, the dominant current component is due to
(a) drift
(b) diffusion
(c) drift and diffusion both
(d) leakage current of drain source p-n junctions.

(vi) In degenerately doped n-type semiconductor the Fermi level lies in the
(a) middle of the bandgap
(b) conduction band
(c) between the donor level and the conduction band
(d) below the donor level.

(vii) The process of adding impurities to a pure semiconductor is called
(a) mixing (b) doping
(c) diffusing (d) none of the above.

(viii) In a metal
(a) the electrical conduction is by electrons and holes
(b) the conductivity decreases with the rise in temperature
(c) the conduction band is empty
(d) none of the above.

(ix) MOSFET uses the electric field of
(a) gate capacitance to control the channel current
(b) barrier potential of p-n junction to control the channel current
(c) both (a) and (b)
(d) none of these.

(x) Velocity saturation in a short channel device causes the drain current to saturate at
(a) same Vds (b) lower Vds
(c) Higher Vds (d) Vt.

Group – B

2. (a) What is built-in potential of a p-n junction?

(b) Draw the charge distribution profile of an abrupt p-n junction. Using the depletion approximation obtain the electric field profile in this structure. Describe the nature of variation of depletion layer width with the applied bias and doping concentration.

3 + (2 + 5 + 2) = 12

3. (a) Draw the schematic cross section of n-MOS capacitor and energy band diagram under different bias conditions.

(b) Explain surface scattering in MOSFET and how it is dependent on gate voltage.

(c) What is the influence of halo implant in the MOS structure for SCE reduction?

4 + 4 + 4 = 12

Group – C

4. (a) Derive the drain current expression of a long channel n-MOSFET and explain the different regions of the I-V characteristics.

(b) What is Gradual Channel Approximation? Discuss the conditions for which this approximation is valid.

8 + (2 + 2) = 12

5. (a) What is heterojunction? Compare homojunction and heterojunction using schematic diagram.

(b) Explain how 2DEG formation in MOSFET. Compare 2DEG in heterojunction and MOSFET.

(c) Explain the operation of a high electron mobility transistor (HEMT) with the help of necessary illustration.

3 + 5 + 4 = 12

Group – D

6. (a) Why do we need to scale down V_{dd} to minimize DIBL effect? What will be the effect of V_{dd} scaling on the device?

(b) Explain the advantages and disadvantages of underlap MOSFET structure.

(c) How the on current in the underlap MOSFET structure is improved by gate metal work function engineering?

4 + 4 + 4 = 12

7. (a) How substrate doping influences SCE?

(b) What are the advantages of a SOI MOSFET structure?

(c) Draw the cross-sectional diagram of a planar DG-MOSFET and explain how it is better compared to an FD-SOI device.

(d) Why undoped substrate is chosen for scaled double-gate MOSFET?

2 + 3 + 5 + 2 = 12

Group – E

8. (a) Write down the threshold voltage expression of a long channel MOSFET and describe each of the terms in the expression.

(b) Derive an expression for the threshold voltage of a short channel MOSFET considering the charge sharing model.

4 + 8 = 12

9. (a) What are the sources of parasitic capacitances in the MOSFET? Draw the small signal equivalent circuit of the MOSFET and show the parasitic elements in the circuit.

(b) Discuss the importance of Pao-Sah integral formula for modelling carrier transport in MOSFET.

(c) What is the relationship between the parasitic capacitance and the cut off frequency of the MOSFET?

5 + 4 + 3 = 12