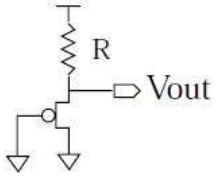
(v) What has been considered as the industry standard of linear ICs?
(a) 555 timer (b) 741 op amp
(c) LM 340 (d) LM 317.

(vi) What is the typical input bias current of a 741 operational amplifier?
(a) 70 nA (b) 80 nA
(c) 90 nA (d) 100 nA.

(vii) What is the most common method used for the growth of single crystals for IC fabrication?
(a) Epitaxial growth (b) Czochralsky pulling technique
(c) Film deposition (d) Photolithography.

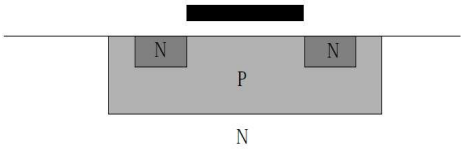
(viii) In the figure below, assuming that the resistance R is very large, what is the best approximation for V_{out}?



(a) $-V_{tp}$ (b) V_{DD} (c) $V_{DD}-V_{tp}$ (d) 0.

(ix) Basic building block in digital circuit is/are
(a) NAND (b) NOR
(c) AND (d) both (a) and (b).

(x) The MOSFET below



is labeled with the different types of silicon. The device is best described as
(a) an NFET in an N-well (b) an NFET in a P-well
(c) a PFET in an N-well (d) a PFET in a P-well.

Group – B

2. (a) Briefly describe the steps associated in IC processing, fabrication and packaging.

(b) Write short note on MOS based active resistor circuit.

8 + 4 = 12

3. (a) Derive an expression for propagation delay in a CMOS inverte capacitor load. Comment on the relation between propagation and capacitance of the load.

(b) For a 0.25µm process characterized by V_{DD}=2.5V, V_{tn}= - V_{tp} k'_n=3.5k'_p=115 µA/V², find t_{PLH}, $t_{PHL}$and t_P for an inverter $(W/L)_n$=1.5, $(W/L)_p$=3 and C=10fF.

6 +

Group – C

4. (a) Derive the expression of dominant pole frequency (f_p), unity bandwidth (f_t) and slew rate (SR) of 741 op-amp. How are related to each other?

(b) What is the use of 741 op-amp output short circuit prot circuit?

(6 + 2) +

5. (a) Perform small signal analysis on a MOS cascode amplifier w the load circuit and derive an expression for voltage gain and c resistance.

(b) It is required to connect a transducer having an open-circuit v of 1V and source resistance of 1MΩ to a load of 1kΩ resistance the load voltage if the connection is done (i) directly and (ii) th a unity gain voltage follower.

6 +

Group – D

6. (a) Briefly explain the operation of charge-redistribution Anal Digital Converter.

(b) Consider a 5-bit charge redistribution A/D converter with V_{REF} What is the full scale voltage of this converter?

10 +

7. (a) Obtain the expressions for common mode gain and CMRR f active loaded MOS differential pair.

(b) An active loadedMOS differential amplifier has the following specifi $(W/L)_n$=100, $(W/L)_p$=200, $\mu_n C_{ox}$=2$\mu_p C_{ox}$=0.2mA/V², V_{An}=|V_{Ap} I_0=0.8mA, R_{ss}=25KΩ. Calculate G_m, R_o, A_d, $|A_{cm}|$, and CMRR.

7 +

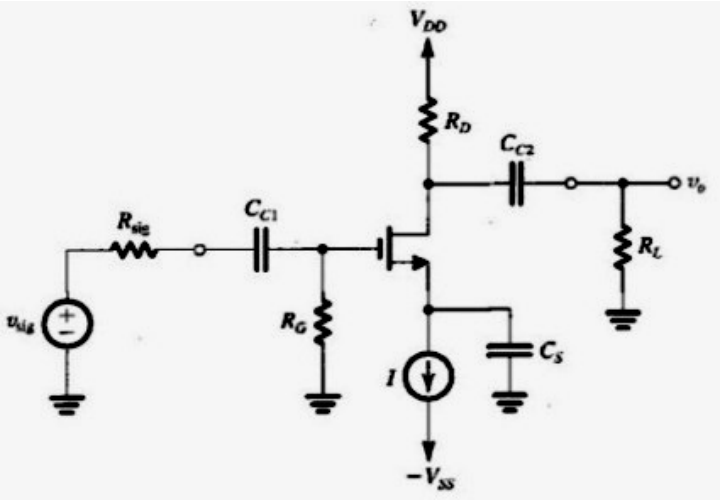
Group – E

8. (a) Briefly explain the CMOS realization of AOI gate and explain with truth table.

   (b) Implement $F = \overline{AB + \overline{AB}}$ using the AOI logic gate.

8 + 4 = 12

9. (a) Perform small signal analysis on the given NMOS amplifier circuit, shown in the following figure. Find an expression for output impedance and voltage gain.



   (b) Compare a bipolar current mirror with MOS mirror. What is bias compensation in a bipolar mirror and how does it improve current transfer ratio.

4 + 8 = 12

MICRO ELECTRONIC DEVICES AND CIRCUITS (AEIE 5101)

Time Allotted : 3 hrs **Full Marks :**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group

Candidates are required to give answer in their own words as far a practicable.

Group – A
(Multiple Choice Type Questions)

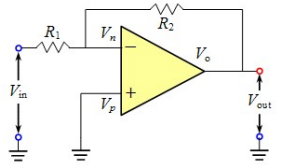
1. Choose the correct alternative for the following: **10 × 1**

   (i) The threshold voltage of an n-channel MOSFET can be increase
   (a) increasing the channel dopant concentration
   (b) reducing the channel dopant concentration
   (c) reducing gate oxide thickness
   (d) reducing the channel length.

   (ii) In a CMOS inverter the upper MOSFET is
   (a) active load (b) passive load
   (c) complementary load (d) none of the above

   (iii) The extremely high input impedance of a MOSFET is primarily due
   (a) absence of its channel
   (b) negative gate-source voltage
   (c) depletion of current carriers
   (d) extremely small leakage current of its gate capacitor.

   (iv)



   If R_1 = 10 kΩ, and R_2 = 30 kΩ, the input impedance of the circuit
   (a) 10kΩ (b) 40kΩ
   (c) infinity (d) none of the above