(vii) Both Power and Delay Reduction for a Digital Gate is possible if
(a) C_L Decreases (b) V_{DD} Decreases
(c) Activity Factor Decreases (d) Never Possible

(viii) If C_L Load Capacitance of Digital Gate increases, below power decreases
(a) Leakage (b) Dynamic
(c) Short Circuit (d) None of above

(ix) If Keeper Size of Dynamic Gate is increased
(a) delay Increases (b) noise Increases
(c) no change in delay (d) no change in noise

(x) If Rise Time of input of a inverter is increased, then Short Circuit Current
(a) increases linearly (b) decreases linearly
(c) remains Same (d) decreases exponentially

Group - B

2. (a) If P_A and P_B are Signal Probability of A and B input of a NAND gate, calculate Transition Probability of output Y of NAND gate.

(b) Explain Glitch Power of a Digital Circuit with an example and show how that can be reduced with same example.

6 + 6 = 12

3. (a) Under what input condition Channel Leakage Power through a 3 input NAND Gate is minimum and why?

(b) Draw Gate Delay vs Threshold voltage curve for various Supply Voltages of a digital Gate and explain.

6 + 6 = 12

Group - C

4. (a) What are various techniques of Dynamic Power reductions by changing Power Supply (V_{DD}).

(b) Define Short Circuit Power in VLSI Circuit and Explain short Circuit Power Reduction Techniques.

6 + 6 = 12

5. (a) Why High K plus Metal gate Transistor was introduced from 45nm onwards?

(b) How FINFET can save more channel and gate leakage with respect to traditional MOS Transistor for similar performance.

6 + 6 = 12

Group - D

6. (a) Explain how Multiple Threshold Voltage devices can reduce leakage power significantly without compromising chip frequency.

(b) For 3 input NOR gate, mention leaking transistors (channel leakage) for all possible combination of inputs including stacking effect.

6 + 6 = 12

7. (a) What is Short Circuit Power in VLSI Circuit and how short Circuit Power can be reduced ?

(b) Which architecture is better between parallel and pipeline architecture from power and area perspective assuming same throughput and why? Explain with example.

6 + 6 = 12

Group - E

8. (a) Draw Circuit Diagram of 6 Transistor SRAM cell with appropriate interface signals and show sources of various leakage power in SRAM cell?

(b) Why pseudo NMOS logic family is not power friendly?

6 + 6 = 12

9. (a) Why Dynamic Power in memory array is not as critical as data-path circuit ?

(b) How Feed forward inverter in Keeper Circuit can save power of a dynamic logic gate?

6 + 6 = 12

M.TECH/ECE(VLSI)/2ND SEM /VLSI 5241/2016
2016

LOW POWER VLSI CIRCUIT AND SYSTEM
(VLSI 5241)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) Maximum Power saving is possible in
(a) System Level (b) Architecture Level
(c) Transistor Level (d) Gate Level

(ii) From 65nm Onwards below power is maximum in a chip
(a) Dynamic (b) Leakage
(c) Short Circuit (d) Contention

(iii) If Threshold Voltage of transistor is increased, Channel Leakage of transistor
(a) decreases linearly (b) increases linearly
(c) decreases exponentially (d) remains same

(iv) If P_A is Signal Probability of a input of Buffer, The Signal Probability of Buffer Output is
(a) P_A (b) $1-P_A$ (c) 1 (d) 0.25

(v) Memory Cell with Maximum leakage is
(a) SRAM Cell (b) DRAM Cell
(c) Latch Cell (d) Flip Flop Cell

(vi) Maximum Leakage reduction in ROM array is possible with
(a) all '0' bits in array (b) all '1' bits in array
(c) 50% '0' bits in array (d) 75% '0' bits in array