(vi) In case of underlap DG MOSFETs, the GIDL current
(a) increases (b) decreases
(c) doubles (d) is unchanged.

(vii) The extremely high input impedance of a MOSFET is primarily due to the
(a) absence of its channel
(b) negative gate-source voltage
(c) depletion of current carriers
(d) extremely small leakage current of its gate capacitor

(viii) The main factor which makes a MOSFET likely to breakdown during the normal handling
(a) very low gate capacitance
(b) high leakage current
(c) high input resistance
(d) both (a) and (c)

(ix) Lateral channel engineering or HALO implant causes
(a) reduction of DIBL effect (b) lowering of Vth roll off
(c) increased RSCE (d) all of the above

(x) Graphene is a _____ band gap semiconductor.
(a)zero (b) wide (c) low (d) infinite.

Group – B

2. (a) How a step potential profile can be created along the channel of the MOSFET using work function engineering?

(b) Explain the effect of higher work function gate material near the drain side of the device.

(c) Explain how the use of dual material gate can control the on current and DIBL of the conventional DG MOSFET?

4 + 3 + 5 = 12

3. (a) How substrate doping influences SCE?

(b) Draw the cross-sectional diagram of a planar DG-MOSFET and explain how it is better compared to an FD-SOI device.

(c) Why undoped substrate is chosen for scaled double-gate MOSFET?

2 + 5 + 5 = 12

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Group – C

4. (a) Explain gate tunneling currents. Why does gate tunnelling occur in a device?

(b) Explain how gate tunnelling current can be overcome by the use of high k dielectric material?

(c) What are the limitations of using high k dielectric material?

5 + 5 + 2 = 12

5. (a) Explain the problem associated with polysilicon gate and metal gate.

(b) What do you mean by polysilicon depletion effect?

(c) What do you mean by surface scattering?

(d) Write a short note on PD-SOI and FD-SOI MOS structure?

3 + 2 + 3 + 4 = 12

Group – D

6. (a) Discuss corner effects in Triple Gate FinFETs. How can they be taken care of in these structures?

(b) What is device width quantization problem in FinFETs?

(c) Write a short note on volume inversion in DG MOSFETs.

4 + 4 + 4 = 12

7. (a) What is process variability in CMOS technology? Why is its study important?

(b) Explain how the High-K dielectric morphology introduces significant process variability.

6 + 6 = 12

Group – E

8. (a) What is modulation doping? What are its benefits?

(b) Explain how modulation doping is used in MODFETs.

(2+2) + 8 = 12

9. (a) Discuss in brief, some of the interesting properties of Graphene that make it a subject of consideration for novel devices.

(b) Write a short note on graphene nanoribbons.

6 + 6 = 12

2016

ADVANCED MICRO & NANO DEVICES
(VLSI 5231)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

(i) The expression [$I_D=k(V_{gs}-V_{th})^2$] can be used only for
(a) BJT (b) E-MOSFET (c) D-MOSFET (d) JFET

(ii) In comparison to conventional bulk MOSFETs, in SOI devices the body effect is
(a) high (b) low (c) absent (d) same

(iii) The transit time of the current carriers through the channel of a JFET decides it's ……..characteristics
(a) source (b) drain
(c) GATE (d) source and drain

(iv) An E-MOSFET that operates at the cutoff or in the ohmic region is an example of
(a) Current source (b) An active load
(c) A passive load (d) A switching device

(v) 2DEG results in high mobility because
(a) there is negligible impurity scattering
(b) there is no scattering
(c) electrons are in a quantum well
(d) none of these.