(iv) One of the disadvantages of the switched capacitor circuits is
(a) the necessity of bandwidth of the signal being equal to the clock frequency
(b) the necessity of bandwidth of the signal being less than the clock frequency
(c) the necessity of bandwidth of the signal being greater than the clock frequency
(d) the necessity of bandwidth of the signal being exactly double the clock frequency

(v) The slew rate of the op amp is determined by
(a) Maximum current available to charge or discharge capacitance.
(b) Settling time
(c) Current sourcing / sinking capability of the first stage
(d) Both (a) & (c)

(vi) The gate-to-channel capacitance of the MOSFET is given as,
(a) $C_{GC}=W_{eff}(L-LD)C_{ox}$ (b) $C_{GC}=W_{eff}(L-LD)C_{ox}$
(c) $C_{GC}=W_{eff}(L+LD)C_{ox}$ (d) $C_{GC}=W_{eff}LC_{ox}$
Where, LD stands for the lateral diffusion component.

(vii) A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101.
(a) 0.3125 V (b) 3.125 V (c) 0.78125V (d) -3.125 V

(viii) In a sample-and-hold circuit, the minimum sample-and-hold time is
(a) $T_{sample}=t_{settling}+t_{acquisition}$ (b) $T_{sample}=t_{settling}$
(c) $T_{sample}=t_{acquisition}$ (d) $T_{sample}=t_{settling}+t_{acquisition}+T_{clock}$

(ix) The current mirror can behave differently from the ideal situation due to
(a) channel length modulation effect
(b) threshold offset between two transistors
(c) imperfect geometrical matching
(d) all of the above

(x) What is the conversion time of a flash converter?
(a) 20μs (b) 1μs
(c) 2μs (d) conversion takes place continuously





**Group - B**

2. (a) What do you understand by the small-signal analysis of the circuit? Explain the purpose of dc model and small-signal modelling of the device?

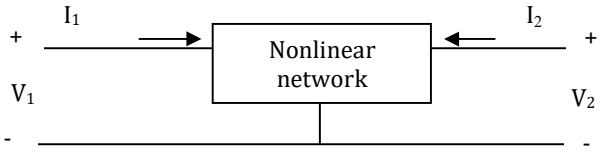

Fig. 1.

(b) The mathematical relationship between the variables $V_1$, $V_2$, $I_1$, and $I_2$ shown in Fig. 1 is given by the following equations, $V_1=I_1R_1$ and $I_2= I_0e^{k1V1}+(V_2/R_2)$, for $V_1>0$ and $I_2=k_2V_1^2+I_0+(V_2/R_2)$, for $V_1<0$.
(i) Determine the small signal model of the network for $V_1>0$.
(ii) Determine the small signal model of the network for $V_1<0$.
(iii) Draw the small signal equivalent circuit if the device is biased to operate at a quiescent value of $I_1$=10 mA and $V_2$=4 V. Assume $I_0$=5 mA, $k_1$=0.2 $V^{-1}$, $k_2$=3 mA/$V^2$, $R_1$=2 KΩ and $R_2$=4 KΩ.

**(2+4) + 6 = 12**

3. (a) Explain the large-signal model for the MOS transistor.

(b) Explain the dependence of gate-to-source, gate-to-drain, and gate-to-bulk capacitance on the gate-to-source voltage for zero body-to-source voltage and constant drain-to-source voltage.

**5 + 7 = 12**

**Group - C**

4. (a) Explain the data conversion mechanism in an *N*-bit pipeline algorithmic analog –to-digital converter.

(b) If the sampled analog input to a 4-bit pipeline algorithm ADC is 2 Volts and $V_{REF}$ = 5 Volts, then evaluate the digital output word and the analog equivalent voltage. Show that the ADC will have an error in the fifth bit if the gain of the first stage is 1.875 when $V_{IN} = V_{REF}$.

**5 + (5+2) = 12**

5. (a) Find the expression of the SNR of the digital-to-analog converter and define the ENOB.

(b) Explain the working principle of the current scaling DAC implemented using binary weighted current sinks.

**(4+2) + 6 = 12**

**Group - D**

6. (a) Discuss the effects of nonlinearity in RF circuits. An analog multiplier "mixes" its two inputs $x_1(t)$ and $x_2(t)$, ideally producing output $y(t) = kx_1(t)x_2(t)$, where $k$ is a constant. Assume $x_1(t) = A_1 \cos\omega_1 t$ and $x_2(t) = A_2 \cos\omega_2 t$.
   (i) If the mixer is ideal, determine the output frequency components.
   (ii) If the input port sensing $x_2(t)$ suffers from third-order nonlinearity, determine the output frequency components.

   (b) Explain the phenomenon of cross-modulation.
   If an interferer contains phase modulation but not amplitude modulation, does cross modulation occur in this case?

**(3+4) + (2+3) = 12**

7. (a) Explain the "current crowding" effect in spiral inductors.

   (b) Estimate the power loss in the substrate using a distributed model of a spiral inductor.

**6 + 6 = 12**

**Group - E**

8. (a) Draw the circuit of a continuous time integrator. Explain how the discrete-time counterpart of this circuit is developed for sampled data systems with neat diagrams.

   (b) Discuss the drawbacks of the discrete –time integrator circuit.

**(2+6) + 4 = 12**

9. (a) Why switched capacitor circuits are preferred for implementing analog signal processing circuits? Draw the configuration of a series-parallel switched capacitor equivalent resistor and emulate its equivalent resistance.

   (b) For this configuration, find out the capacitor C (considering $C_1=C_2=C$) that can emulate a 1 MΩ resistor if the clock frequency is 250 KHz.

**(2+8) + 2 = 12**





**2016**

# ANALOG IC DESIGN
# (VLSI 5203)

**Time Allotted : 3 hrs** **Full Marks : 70**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

## Group – A
## (Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1=10**

   (i) An ideal differential amplifier should have
   (a) CMRR = 0 (b) CMRR = 1
   (c) CMRR > 1 (d) CMRR = ∞

   (ii) Cascode amplifiers
   (a) Increases the effect of Miller capacitance on the input of the amplifier
   (b) Reduces the effect of Miller capacitance on the input of the amplifier
   (c) Reduces the effect of Miller capacitance on the output of the amplifier
   (d) None of the above.

   (iii) For a good design of the MOSFET, the relationship between the thermal noise arising from the gate resistance and the channel should satisfy
   (a) $4kT\frac{R_G}{3} << \frac{4kT\gamma}{gm}$ (b) $4kT\frac{R_G}{3} >> \frac{4kT\gamma}{gm}$
   (c) $4kT\frac{RG}{3} = \frac{4kT\gamma}{gm}$ (d) None of the above.