(vii) ATPG is based on
(a) Stuck at fault (b) BIST
(c) Bridging fault (d) DFT

(viii) Signature analyser (SA) is part of
(a) Scan Design (b) Boundary Scan
(c) BIST (d) Ad hoc DFT

(ix) With Technology advancement via contact resistance
(a) increases (b) decreases
(c) remains same (d) hard to say

(x) Setup margin for a path is +10ps for Cycle Time of 200ps. If Cycle time is reduced to 180ps, then new setup margin for the path will be
(a) +40ps (b) +10ps
(c) 0ps (d) -10ps

Group – B

2. (a) Explain various components of a Memory Block with diagram.

(b) For a Memory Block of 16K Memory Locations and 16 Data bits, explain how many row address bits and how many column address bits are needed.

6 + 6 = 12

3. (a) What is input test pattern to detect Stuck-at-1 fault at the Output of a 2 input NAND gate?

(b) Explain D-Algorithm using an example.

6 + 6 = 12

Group – C

4. (a) For a flip flop based sequential circuit, Cycle Time = 100ps, Setup Time = 25ps, Clock-Skew = 10ps, Combinational Delay = 60ps, Clock to Out Delay of Flop = 20ps. Hold Time = 40ps. What is setup margin and hold margin for the Circuit?

(b) Define clock skew and what are sources of Clock Skew?

6 + 6 = 12

5. (a) As per Process Technology, Metal-6 resistance is 100mohms/um and capacitance is 0.2ff/um. If 1mm wire is routed using Metal-6, draw

circuit diagram of 3 segment pi model with appropriate resistance and capacitance value of individual segments.

(b) Why driver side of a wire needs to be low resistance and receiver side of the wire needs to be low capacitance, explain using Elmore Delay model.

6 + 6 = 12

Group – D

6. (a) Explain write '1' followed by read '1' operation in 1-Transistor DRAM Circuit using circuit diagram and timing waveforms.

(b) Explain sizing criteria of 6 Transistor SRAM cell.

6 + 6 = 12

7. (a) Explain H-Tree of clock distribution using circuit diagram.

(b) Explain transparency of a D-Latch with circuit diagram and timing waveforms.

6 + 6 = 12

Group – E

8. (a) Why post Si debug is needed ?

(b) Explain D-Algorithm with a circuit example.

6 + 6 = 12

9. (a) Using Circuit diagram explain how Level Sensitive Scan Design Flip Flop (LSSD-SFF) works.

(b) Explain Scan Design Methodology with flow diagram.

6 + 6 = 12

M.TECH/ECE(VLSI)/2ND SEM /VLSI 5202/2016
2016

VLSI DESIGN, VERIFICATION AND TESTING
(VLSI 5202)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 × 1=10**

(i) Yield Y = 99% and Fault Coverage T = 90%, DPM (Defects Per Million) is
(a) 10000 (b) 10,00 (c) 28,000 (d) 50,000

ii) Scan Design is needed to test
(a) Sequential Circuit (b) Combinational Circuit
(c) Stuck at Faults (d) none of above

(iii) Memory with multiple read and write port is
(a) DRAM (b) ROM (c) Register File (d) SRAM.

(iv) Interruptible Keeper Latch has issue with
(a) noise only (b) delay only
(c) both delay and noise (d) none of above

(v) Wire RC model acts as
(a) High pass filter (b) Low pass filter
(c) Band pass filter (d) All pass filter

(vi) In which of the following Memory Array architectures fastest memory access happens?
(a) DRAM (b) SRAM
(c) Hard Disk (d) Register File