(vi) Stall in pipelining is
(a) delay in execution of an instruction
(b) first stage of pipelining
(c) speed up execution of an instruction
(d) none

(vii) A ---------- is a function that, when applied to a particular computer state generates next state.
(a) Filter (b) State (c) Command (d) Program.

(viii) An hardware accelerator is
(a) an active filter (b) not a co-processor
(c) same as a co-processor (d) a passive filter

(ix) ALU is the basic unit used in designing which stage of pipelining
(a) Instructions Fetch (b) Instruction Decode
(c) Execution (d) none

(x) How many operating modes are there in ARM processor?
(a) five (b) six (c) seven (d) eight.

Group - B

2. (a) Discuss about the different hazards in pipelining.

(b) Assuming no result forwarding and the five stage sample pipeline, draw a pipelined execution diagram for the following code fragment:
ADD r_1, r_2, r_3
SUB r_4, r_5, r_6
MUL r_8, r_9, r_{10}
DIV r_{12}, r_{13}, r_{14}

4 + 8 = 12

3. (a) Give the classification of the vector instructions.

(b) Indicate the different fields by which vector instructions are usually specified.

(c) Give the block diagram to indicate the architecture of a typical vector processor with multiple function pipes.

2 + 5 + 5 = 12

Group - C

4. (a) Compare the fixed point and floating point DSP processor?

(b) Illustrate the function of ALU, accumulators, barrel shifter, multiplier/adder and CSSU unit for TMS320C54xx digital signal processor.

5 + 7 = 12

5. (a) Is VLIW architecture now just limited to DSP processor? If not, have there been any new VLIW chip released for other workloads. What is the difference between VLIW & EPIC?

(b) List the different buses of TMS320C5X and their functions.

(c) Describe the functional units in CALU of TMS320C5X with a diagram and explain the source and destination of operands of each of these units.

4 + 3 + 5 = 12

Group - D

6. (a) Define the accelerator in computer architecture. Why we need accelerator in the architecture, illustrate with an example.

(b) Draw the block diagram of accelerator attached with base processor through bridge or without bridge interconnect.

(3+3) + (3+3) = 12

7. (a) In what ways classify the processors in embedded system? What are the points to be considered while connecting power supply rails with embedded system?

(b) Compare ARM Multicore processors Cortex A, Cortex R, Cortex-M, and Secure Core and their applications.

(c) Give a detailed description of ARM Cortex A8 with block diagram.

3 + 5 + 4 = 12

Group - E

8. (a) What are the differences between fine and coarse grain multi threading?

(b) Explain how the simultaneous multithreading (SMT) improves the efficiency of the superscalar processor.

(c) What are the benefits of processor customization using system on chip design.

3+5+4 = 12

9. (a) Compare CMP (Chip Multiprocessors) with multichip multiprocessors.

(b) Issustrate the features of FPGA core. What do you mean by PSoC?

(c) What is the difference between a SOC setup and a microcontroller design?

3 + (3+2) + 4 = 12

2016

VLSI PROCESSOR ARCHITECTURE
(VLSI 5201)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following: **10 × 1=10**

(i) ARM processor is a
(a) RISC (b) CISC (c) VLIW (d) DSP processor.

(ii) The basic principle of Harvard Architecture is
(a) Storing both the Program and the Data in the same Memory
(b) Storing Program and the Data segments in separate Memory
(c) Using super pipelining VLIW concept
(d) Using CISC architecture

(iii) The Micro-instructions are stored in
(a) Main Memory (b) Cache memory
(c) Flash memory (d) Control Memory

(iv) Architecture that has ability to simultaneously issue three operations
(a) SISD (b) VLIW (c) RISC (d) CISC

(v) If two instructions in a pipeline are waiting on a Multiplier unit to become available, then the associated pipeline hazard type is
(a) Resource (b) Data
(c) Control (d) Floating Point