ANALOG VLSI IC DESIGN
(VLSI 5201)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Charge injection phenomenon in MOS switch is dominant when
(a) MOS switch turns on (b) MOS switch turns off
(c) Both (a) and (b) (d) None of the above.

(ii) The highest value of Input Common-Mode Range (*ICMR*) of a differential amplifier is limited by the requirement that
(a) both MOSFETs should be in saturation region
(b) both MOSFETs should be in triode region
(c) one MOSFET should be in saturation & another in triode region
(d) one MOSFET should be in saturation & another in deep triode region.

(iii) Switched capacitor circuits are
(a) Discrete in amplitude and discrete in time
(b) Discrete in amplitude and continuous in time
(c) Continuous in amplitude and discrete in time
(d) Continuous in amplitude and continuous in time.

(iv) The resistance between the drain and source terminal is proportional to
(a) λ^2 (b) λ (c) λ^{-1} (d) λ^{-2}

(v) The ENOB of a DAC is defined as
(a) $(SNR_{actual} - 1.76) / 6.02$ (b) $(SNR_{max} - 1.76) / 6.02$
(c) $(SNR_{actual} + 1.76) / 6.02$ (d) $(SNR_{max} + 1.76) / 6.02$

(vi) The error tolerance at the output of S/H (Sample / Hold) depends on the amplifier's
(a) Offset (b) Gain Error
(c) Linearity (d) All of the above.

(vii) The small-signal condition for an N-channel enhancement MOSFET amplifier is given by
(a) $v_{gs} << V_{ov}$ (b) $v_{gs} << (V_{ov}/2)$ (c) $v_{gs} << 2V_{ov}$ (d) $v_{gs} = V_{ov}$

(viii) The backgate transconductance (g_{mb}) obtained in the small-signal analysis of the MOSFET depends on
(a) Body coefficient only
(b) Back gate bias only
(c) Body coefficient and back gate bias both
(d) None of the above.

(ix) The frequency of the signal applied to the switched-capacitor circuit should satisfy the criteria
(a) $f_{signal} << f_{clock}$ (b) $f_{signal} >> f_{clock}$
(c) $f_{signal} = 2f_{clock}$ (d) $f_{clock} = 2f_{signal}$

(x) Integrated transmission line (T-line) structures include
(a) Microstrip Line (b) Stripline
(c) Coplanar Lines (d) All of the above.

Fill in the blanks with the correct word

(xi) Source/Drain terminals are interchangeable since MOSFET is a _____ device.

(xii) The full form of SFDR is _____ .

(xiii) The unit _____ refers to 'dB's above 1mW'.

(xiv) Switched-capacitor circuits are _____ sampled data circuits.

(xv) An ideal differential amplifier should have common-mode voltage gain _____.

Group - B

2. (a) What do you understand by small-signal analysis? *[(CO2)(Understand/LOCQ)]*
(b) Derive the voltage gain of a symmetric resistive load differential amplifier from its small-signal equivalent circuit. *[(CO2)(Analyze/IOCQ)]*
(c) The circuit in *Fig. 1* uses a resistor rather than a current source to define a tail current of 1 mA. Assume, $(W/L)_{1,2} = (25 / 0.5)$, $\mu_n C_{OX} = 50\ \mu A/V^2$, $V_{th} = 0.6\ V$, $\lambda = \gamma = 0$, and $V_{DD} = 3\ V$. Evaluate the required input common mode (CM) for which R_{SS} sustains *0.5 V*. Also calculate R_D for a differential gain of *5*.

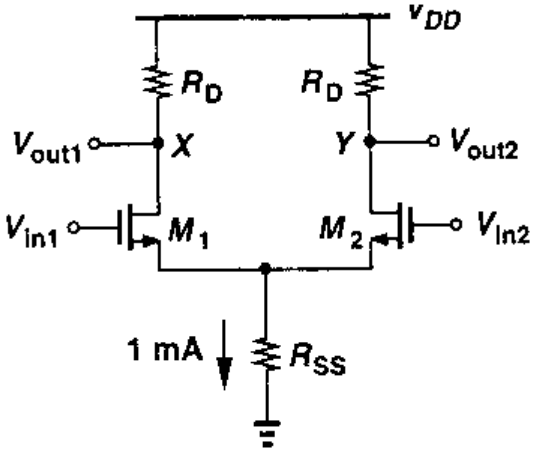

Fig. 1 *[(CO2)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

3. (a) Briefly discuss the limitations of MOS switch. *[(CO1)(Understand/LOCQ)]*
(b) Draw and explain the small-signal equivalent circuit of MOS switch. *[(CO1)(Analyze/IOCQ)]*

(c) Is "Dummy Transistor" technique equally effective to overcome all types of MOS switch limitations? Justify your answer. *[(CO1)(Analyze/IOCQ)]*

4 + 5 + 3 = 12

Group - C

4. (a) Briefly discuss the "Skin Effect". *[(CO3)(Understand/LOCQ)]*

(b) Model the parasitic capacitance and hence estimate the total energy stored in the spiral inductor structure. *[(CO3)(Analyze/IOCQ)]*

(c) An engineer wishes to design a spiral inductor for a 900 MHz GSM system. Determine if the 5 nH structure is suited for this application. *[(CO3)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

5. (a) Briefly explain the dynamic range and SFDR. *[(CO3)(Understand/LOCQ)]*

(b) The upper end of the dynamic range is limited by intermodulation in the presence of two interferers or desensitization in the presence of one interferer. Compare these two cases and determine which one is more restrictive. *[(CO3)(Apply/IOCQ)]*

(c) A broadband circuit sensing an input $V_0Cos\omega_0t$ produces a third harmonic $V_oCos(3\omega_0t)$. Determine the *1-dB* compression point in terms of V_0 and V_3. *[(CO3)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

Group - D

6. (a) Briefly explain the working principle of pipeline algorithmic ADC. *[(CO4)(Analyze/IOCQ)]*

(b) Assume that the sampled analog input to a *4-bit* pipeline algorithm *ADC* is *2 volts*. If $V_{REF} = 5$ *Volts*, evaluate the digital output word and the analog equivalent voltage. Show that if $V_{IN} = V_{REF}$, the *ADC* will have an error in the 5^{th} bit if the gain of the first stage is *1.875*. *[(CO4)(Evaluate/HOCQ)]*

(c) Show the signal in time and frequency domain if Nyquist criteria are violated during sampling. *[(CO4)(Apply/IOCQ)]*

4 + 5 + 3 = 12

7. (a) Briefly explain the principle of operation of *R-2R* digital-to-analog converter (*DAC*) circuit. *[(CO4)(Understand/LOCQ)]*

(b) Design a *3-bit DAC* using *R-2R* architecture with $R = 1\ k\Omega$ and $R_F = 2\ k\Omega$ and $V_{REF} = 5V$. Assume that the resistances of the switches are negligible. Determine the value of i_{tot} for each digital input and the corresponding output voltage v_{OUT}. *[(CO4)(Create/HOCQ)]*

(c) Analyze drawbacks of this R-2R ladder architecture, if any. *[(CO4)(Analyze/IOCQ)]*

4 + 6 + 2 = 12

Group - E

8. (a) Briefly explain open-loop and closed loop transfer function with necessary diagram. *[(CO6)(Understand/LOCQ)]*

(b) Can a single common- source stage oscillate if it is placed in a unity gain loop? Justify. *[(CO6)(Apply/IOCQ)]*

(c) Calculate the oscillation frequency and minimum voltage gain per stage of a three-stage ring oscillator. *[(CO6)(Evaluate/HOCQ)]*

4 + 5 + 3 = 12

9. (a) Explain the basic principle of operation of switched-capacitor filters. *[(CO5)(Understand/LOCQ)]*

(b) Emulate the resistor equivalent of a series-parallel switched capacitor circuit. *[(CO5) (Analyze/IOCQ)]*

(c) Design a series-parallel switched capacitor circuit to emulate a *1 MΩ* resistor if *C1 = C2 = C* and the clock frequency is *250 kHZ*. *[(CO5)(Create/HOCQ)]*

4 + 5 + 3 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	29.16	43.75	27.09

Course Outcome (CO):

After the completion of the course students will be able to

[1] Understand and analyze MOS-based analog VLSI sub-circuits, relevant small-signal equivalent circuit models and design them eg. current mirrors

[2] Design and analyze MOS circuits of practical importance eg. common-source amplifiers and differential amplifiers

[3] Understand the basic concepts in RF design and the geometry, models of passive devices used in the RFIC

[4] Understand the principle of operation, characterization of the data converter circuits and design them

[5] Understand and analyze the different topologies of switched-capacitor circuits and apply the concept for the analysis of circuits of practical applications

[6] Understand the principle of operation of the oscillator circuit and apply the concept for the analysis of circuits of practical applications

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*