ADVANCED VLSI PROCESSOR
(VLSI 5241)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) A logic circuit in ALU is
(a) entirely combinational
(b) entirely sequential
(c) both combinational and sequential
(d) purely passive

(ii) RISC machines prefer architecture of type
(a) R+M
(b) R/M
(c) L/S
(d) All of these

(iii) Microinstructions are stored in
(a) Registers
(b) Control memory
(c) Main memory
(d) Flash memory.

(iv) Converting Octal number 7654624 to Hexadecimal give
(a) AB5F51
(b) F18994
(c) 15F994
(d) 1F5994

(v) In the Superpipeline approach the work of _____ pipeline segments are completed in a _____ clock cycle.
(a) multiple, single
(b) single, multiple
(c) single, single
(d) all of these

(vi) A hardware accelerator is
(a) an active filter
(b) same as a co-processor
(c) not a co-processor
(d) a passive filter.

(vii) Multi-core super scalar processor is a
(a) SISD
(b) SIMD
(c) MIMD
(d) MISD.

(viii) The three pipeline data hazards are
(a) RAW,WAR,& WAW
(b) Control, Resource, Data
(c) Store, Memory, Execute
(d) CPU, ALU, GPU.

(ix) _____ is the main property used to achieve higher efficiency with hardware Accelerators
(a) Parallelism
(b) Dependency
(c) Correctness
(d) Preservation

(x) The CMAR (Control Memory Address Register) is used when the CU (Control Unit) design type is
(a) Hard-wired
(b) Micro- Programmed
(c) Firm-wired
(d) Soft-wired.

Fill in the blanks with the correct word

(xi) In ARM processor R14 is _____ _____ and R15 is _____ _____.

(xii) A CMP (Chip Multiprocessor) is a group of _____integrated onto the same processor, while a SOC (System on Chip) integrates all components of an _____ system into a single chip.

(xiii) TMS320C5X DSPs are said to have advanced _____ architecture because they have _____memory bus structures for program and data.

(xiv) In a multicore processor multiple _____ cores coexist on single processor chip.

(xv) Single Pipeline Processors are categorized under _____.

Group - B

2. (a) What is pipelining? What are the advantages of a pipelined CPU? *[(CO1)(Understand/LOCQ)]*

(b) What is the drawback of static pipelining? *[(CO1)(Understand/LOCQ)]*

(c) If the number of stages in a pipelined hardware unit is K, prove that the throughput gain would be K times. *[(CO1)(Apply/IOCQ)]*

(d) What is Harvard architecture? What is its usefulness? *[(CO2)(Remember/LOCQ)]*

(3 + 3) + 2 + 2 + (1 + 1) = 12

3. (a) Explain the differences between the RISC and the CISC processors. *[(CO2)(Understand/LOCQ)]*

(b) Explain the work of microinstruction using control memory, control address register, control buffer, and sequencer logic *[(CO1)(Remember/LOCQ)]*

(c) A non pipeline takes 40ns to complete a task. The same task can be processed in 4 segment pipeline with a clock cycle of 4ns. Determine the speed up ratio of the pipe line for 50 tasks. What is the maximum speed up that can be achieved in this case? *[(CO1)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) Explain how a higher throughput is obtained using the VLIW architecture. Give an example, of a DSP that has VLIW architecture. *[(CO3)(Understand/LOCQ)]*

(b) What are the various interrupt types supported by the TMS320C5X processor? *[(CO3)(Remember/LOCQ)]*

(c) Let the content AR0 be 2345h and the content of data memory location 1500h be 6789h, before executing the instruction SMMR AR0, #1500h. After executing the instruction, what will be contents of AR0 and the data memory location? *[(CO3)(Apply/IOCQ)]*

5 + 3 + 4 = 12

5. (a) Explain how convolution is performed using a single MAC unit. *[(CO3)(Remember/LOCQ)]*

(b) What is bit reversed addressing mode? *[(CO3)(Remember/LOCQ)]*

(c) Describe the functional units in CALU of TMS320C5X with a diagram and explain the source and destination of operands of each of these units. *[(CO3)(Understand/LOCQ)]*

4 + 2 + 6 = 12

Group - D

6. (a) What is an hardware accelerator? Explain with example and mention it uses. *[(CO4)(Understand/LOCQ)]*

(b) What is total number of registers in ARM7 processors? Provide the breakup between the general purpose registers, those used under special OS modes, and the status registers. *[(CO5) (Remember/LOCQ)]*

(c) State function of ARM registers R13, R14 and R15. *[(CO5)(Apply/IOCQ)]*

4 + (2 + 3) + 3 = 12

7. (a) State Flynn's Classical taxonomy. Discuss the advantages and disadvantages of shared and distributed memory. *[(CO6)(Understand/LOCQ)]*

(b) Explain with suitable examples the parallelizable problem and the non-parallelizable problem. *[(CO5)(Remember/LOCQ)]*

6 + 6 = 12

Group - E

8. (a) What are the limitations of a uniprocessor? *[(CO6)(Analyse/LOCQ)]*

(b) How does a CMP (Chip Multi Processor) resolve those issues ? *[(CO6) (Remember/LOCQ)]*

(c) A weather forecasting computation requires 250 billion floating point operations. The problem is processed in a supercomputer that can perform 100 mega flops. How long will it take to do these calculations? *[(CO5)(Apply/IOCQ)]*

4 + 4 + 4 = 12

9. (a) Explain with the inter connection network architecture of NUMA and UMA. *[(CO5)(Analyse/LOCQ)]*

(b) What is fine and coarse grained granularity in terms of parallel programming and data usage? *[(CO5) (Remember/LOCQ)]*

(c) Consider a computer with four floating point pipeline processors. Suppose that each processor uses a cycle time of 40 nano sec. How long will it take to perform 400 floating point operations? Is there a difference if the same 400 operations are carried out using a single pipeline with a cycle time of 10 nano secs. *[(CO5)(Apply/IOCQ)]*

4 + 4 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	78.13	21.87	0

Course Outcome (CO):

After the completion of the course students will be able to
1. Students will learn basic structure of instruction set architecture (ISA)
2. Students will learn CISC and RISC Architecture
3. Students will learn sample DSP Processor Architecture
4. Students will learn Accelerator
5. Students will learn Multi-Threaded Processor
6. Students will learn use of Microprocessor cores in SOC Design.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*