ADVANCED NANO DEVICES
(VLSI 5242)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Increase in doping in substrate region of MOSFET will
(a) decrease threshold voltage and increase substrate scattering
(b) decrease threshold voltage and decrease substrate scattering
(c) increase threshold voltage and decrease substrate scattering
(d) increase threshold voltage and increase substrate scattering

(ii) Sub threshold conduction takes place predominantly by
(a) drift
(b) diffusion
(c) both drift and diffusion
(d) tunnelling

(iii) The equivalent oxide thickness when using a high-k-gate dielectric of thickness 10nm and having a dielectric constant of 25 is (given the dielectric constant of SiO_2 to be 3.9):
(a) 1.56nm
(b) 15.6nm
(c) 10nm
(d) 1nm

(iv) A long – channel NMOS transistor is biased in the linear region V_{DS} = 50 mV and is used as a resistance. Which one of the following statements is NOT correct?
(a) If the device width W is increased, the resistance decreases
(b) If the threshold voltage is reduced, the resistance decreases
(c) If the device length L is increased, the resistance increases
(d) If VGS is increased, the resistance increases

(v) Fowler-Nordheim (FN) tunnelling involves the tunnelling of electrons through a
(a) triangular potential barrier
(b) trapezoidal potential barrier
(c) rectangular potential barrier
(d) none of the above

(vi) Consider the following statements for a metal oxide semiconductor field effect transistor (MOSFET): P: As channel length reduces, OFF – state current increases. Q: As channel length reduces, output resistance increases. R: As channel length reduces, threshold voltage remains constant. S: As channel reduces, ON current increases.
Which of the above statements are INCORRECT?
(a) P and Q
(b) P and S
(c) Q and R
(d) R and S

(vii) In a quantum well, the effective energy gap for inter-band transition compared to bulk E_g is
(a) lower
(b) higher
(c) same
(d) none of the above

(viii) The cut off frequency, fT , of the MOSFET is
(a) proportional to transconductance (gm) and inversely proportional to total capacitance between gate to source/drain (Cgs+ Cgd)
(b) proportional to transconductance (gm) and total capacitance between gate to source/drain (Cgs+ Cgd)
(c) inversely proportional to transconductance (gm) and total capacitance between gate to source/drain (Cgs+ Cgd)
(d) inversely proportional to transconductance (gm) and total capacitance between gate to source/drain (Cgs+ Cgd)

(ix) The conduction of current I_D depends on
(i) Gate to source voltage
(ii) Drain to source voltage
(iii) Bulk to source voltage
(iv) Threshold voltage
(v) Dimensions of MOSFET
(a) Only (i)
(b) Only (i), (ii) and (iii)
(c) Only (v)
(d) All of the mentioned

(x) The depletion mode n-MOS differs from enhancement mode n-MOS in
(a) threshold voltage
(b) channel length
(c) switching time
(d) none of the above

Fill in the blanks with the correct word

(xi) Velocity saturation causes the short channel device to saturate for _____ values of V_{DS}.

(xii) Polysilicon granularity is a type of _____ process.

(xiii) A FinFET with multiple fins of number N has an effective device width of _____.

(xiv) Full form of SOI is _____.

(xv) High-K gate dielectric _____ the gate threshold voltage.

Group - B

2. (a) Derive the relationship between threshold voltage and supply voltage. What do you mean by sub-threshold conduction? *[(CO1)(Analyze/IOCQ)]*

(b) What is subthreshold swing? Why subthreshold swing is always higher than 60db/decade for a conventional MOSFET device? *[(CO1)(Analyze/IOCQ)]*

(4 + 2) + (2 + 4) = 12

3. (a) Explain gate tunnelling currents. Illustrate the reason why does gate tunnelling occur in MOSFETs? *[(CO2)(Analyze/IOCQ)]*

(b) List the basic requirements of a high-K oxide. State some limitations of using high-K oxides. *[(CO2)(Evaluate/HOCQ)]*

(2 + 4) + (4 + 2) = 12

Group - C

4. (a) Sketch the small signal equivalent circuit of a MOSFET for high frequency analysis with the inclusion of non-quasi static effects. *[(CO3)(Apply/IOCQ)]*

(b) Derive the cut-off frequency (f_T) of conventional MOSFETs. *[(CO3)(Apply/IOCQ)]*

6 + 6 = 12

5. (a) Justify the incorporation of high-K dielectric materials in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) by discussing their advantages over traditional silicon dioxide (SiO2) dielectrics. *[(CO2)(Evaluate/HOCQ)]*

(b) Explain in details about how high K plus metal gate transistor reduces gate leakage significantly compared to traditional silicon dioxide insulator plus poly gate transistor? *[(CO2)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - D

6. (a) Explain how is FinFET a quasi-planar device? *[(CO4)(Understand/LOCQ)]*

(b) Explain corner effects in Triple-Gate FinFETs. How can they be taken care of in these structures? *[(CO4)(Evaluate/HOCQ)]*

(c) Outline Device-width quantization problem in FinFETs? *[(CO4)(Analyze/IOCQ)]*

4 + 4 + 4 = 12

7. (a) Explain non uniform dopant distribution. Why Double Gate (DG) can improve ON current as well as mitigate OFF current. *[(CO4)(Understand/LOCQ)]*

(b) Why undoped substrate is chosen for scaled DG MOSFETs? *[(CO4)(Analyse/IOCQ)]*

(2 + 6) + 4 = 12

Group - E

8. (a) Discuss the concept of quantization and its significance in the formation of a low-dimensional electron gas in semiconductor structures. *[(CO5)(Remember/LOCQ)]*

   (b) Explain how 2DEG can be formed in the MOSFET. Compare between the 2DEG formed in a MOSFET and in HEMT. *[(CO5)(Analyze/IOCQ)]*

6 + 6 = 12

9. (a) Discuss the significance of flexible electronic devices fabricated on plastic substrates in comparison to rigid counterparts, highlighting their potential applications and advantages. *[(CO6)(Evaluate/HOCQ)]*

   (b) Analyze the role of single-walled carbon nanotubes (SWNTs) in the future of materials science, considering their unique electronic properties and potential applications in molecular electronics. *[(CO6)(Analyze/IOCQ)]*

6 + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	18.75	52.08	29.17

Course Outcome (CO):

After the completion of the course students will be able to :-
1. Students will learn various leakage phenomena in advanced MOS
2. Students will learn High K Plus Metal Gate Technology for advanced Process Nodes
3. Students will learn SOI MOS device
4. Students will learn FinFET Devices like DGMOS, Tri-gate
5. Students will learn Hetero-Structures
6. Students will learn CNT, Graphene Device

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*