COMPUTER ORGANIZATION AND ARCHITECTURE
(CSBS 2202)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) In which addressing the simplest addressing mode where an operand is fetched from memory is _____:
(a) Immediate addressing (b) Direct addressing
(c) Register addressing (d) Indirect addressing

(ii) In booth multiplication algorithm, after the initialization _____ bits (in proper sequence) are inspected.
(a) Qn+1 Qn (b) Qn-1 Qn
(c) Qn Qn-1 (d) Qn Qn+1

(iii) If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10ns memory) is
(a) 93% (b) 90% (c) 88% (d) 87%.

(iv) If the main memory is of 8K bytes and the cache memory is of 2K words. It uses associative mapping. Then each word of cache memory shall be
(a) 11 bits (b) 21 bits (c) 16 bits (d) 20 bits.

(v) Which memory has largest storage capacity among all?
(a) Auxiliary memory (b) RAM
(c) Associative memory (d) Cache memory.

(vi) Which of the following does not use parallel processing?
(a) Pipeline processing (b) Scalar processing
(c) Vector processing (d) Array processors.

(vii) In arithmetic pipeline, what is correct sequence of the sub-operations that are performed in the four segments which are? (1) Normalize the result, (2) Add or subtract the mantissas, (3) Align the mantissas, (4) Compare the exponents
(a) 3, 4, 2, 1 (b) 4, 3, 2, 1 (c) 2, 3, 4, 1 (d) 4, 2, 3, 1.

(viii) Hardware interlocks, Operand forwarding and Delayed load are solutions of which pipeline conflict?

(a) Branch difficulties (b) Resource conflicts
(c) Data dependency (d) Function dependency.

(ix) _____ are the different type/s of generating control signals.

(a) Micro-programmed (b) Hardwired
(c) Micro-instruction (d) Both Micro-programmed and hardwired

(x) SIMD represents an organization that _____.

(a) refers to a computer system capable of processing several programs at the same time
(b) represents organization of single computer containing a control unit, processor unit and a memory unit
(c) includes many processing units under the supervision of a common control unit
(d) none of the above

Fill in the blanks with the correct word

(xi) Both the CISC and RISC architectures have been developed to reduce the _____.

(xii) The average time required to reach a storage location in memory and obtain its contents is called _____.

(xiii) Unit of computer which is capable of performing arithmetic, logical and data manipulation operations on binary numbers is called _____.

(xiv) An address in main memory is called _____.

(xv) In length instruction some programs wants a complex instruction set containing more instruction, more addressing modes and greater address rang, as in case of _____.

Group - B

2. (a) Apply Huffman coding to encode the following instructions and calculate the average length of each instruction.

Instruction	Occurrence Probability
LDA	4/16
ADD	3/16
DIV	1/16
MUL	1/16
STA	4/16
SUB	2/16
BNZ	1/16

[(CO3)(Apply/IOCQ)]

(b) Express the following equation in one address instruction format
x = (a + b) * ((c-d)*e) *[(CO1)(Apply/IOCQ)]*

8 + 4 = 12

3. (a) Multiply the following pairs of signed 2's-complement numbers using the Modified Booth algorithm. Assume that A is the multiplicand and B is the multiplier. A= 010111 and B=110110. *[(CO2)(Apply/IOCQ)]*

(b) "Op-code expansion method increases the number of instruction" – justify with an example. *[(CO1)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - C

4. (a) A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block. Calculate the number of bits in each of the Tag, Set, and Word fields. *[(CO3)(Apply/IOCQ)]*

(b) A memory system contains a cache, a main memory and a virtual memory. The access time of cache is 5 ns and it has an 80% hit ratio. The access time of main memory is 100 ns with a 90% hit ratio. The access time of virtual memory is 10 ms. What is the average access time of the hierarchy? *[(CO3)(Apply/IOCQ)]*

(c) What do you mean by associative mapping? *[(CO3)(Remember/LOCQ)]*

6 + 4 + 2 = 12

5. (a) Explain the importance of TLB with necessary diagram. *[(CO4)(Remember/LOCQ)]*

(b) "Replacement algorithm plays an important role in associative mapping" – justify with an example. *[(CO3)(Evaluate/HOCQ)]*

6 + 6 = 12

Group - D

6. Consider the five-stage pipelined processor specified by the following reservation table (Table 1)

	1	2	3	4	5	6	7	8	9
S1	X					X			X
S2		X			X			X	
S3			X				X		
S4				X					X
S5		X				X			

Table 1

(i) List the set of forbidden latencies and the collision vector.

(ii) Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline.

(iii) List all the simple cycles from the state diagram.

(iv) Identify the greedy cycles among the simple cycles.

(v) What is the minimum average latency (MAL) of this pipeline? *[(CO5)(Apply/IOCQ)]*

(2 + 4 + 2 + 2 + 2) = 12

7. Consider the following instructions set and some assumption for this question:

LD F6, 20(R5)
LD F2, 28(R5)
MULTD F0,F2,F4

SUBD F8,F6, F3
DIVD F10,F0,F6
ADDD F6, F8,F2
SD F8, 50(R5)

(a) Pipeline contains stages: IF, IS (Issue), RO (Read operand), EX and W (Write);
(b) Each stage except EX requires one clock cycle;
(c) System contains 4 Units for FP operations, FP-load / store, FP-addition / subtraction FP-multiplication and FP-division:
i. EX-stage for Load / Store operations contains 1 clock cycle (EX);
ii. EX-stage for ADDD or SUBD operations contains 1 clock cycle;
iii. EX-stage for MULTD operation contains 3 clock cycles;
iv. EX-stage for DIVD operation contains 4 clock cycles;
(d) All memory references hit in cache;
(e) Pipeline has forwarding hardware for all FUs, except FP-Load / Store where operand is ready after W-stage;
i. Draw the Timing diagram of task segment processing.
ii. Point out the different pipeline hazards in the above instructions set and why?
iii. Find out what kind of Data hazards are occurred between the instructions in the above instructions set. *[(CO5)(Apply/IOCQ)]*

(4 + 4 + 4) = 12

Group - E

8. (a) Explain the organization of a microprogrammed control unit with a block diagram. *[(CO6)(Understand/LOCQ)]*
(b) What are the advantages and disadvantages of hardwired and microprogrammed control unit? *[(CO6)(Remember/LOCQ)]*

6 + 6 = 12

9. (a) What is Flynn's Taxonomy? Explain two of them with block diagram. Difference between multiprocessor and multicomputer. What is the benefit of using multiprocessor? *[(CO6)(Understand/LOCQ)]*
(b) Differentiate RISC and CISC architectures. *[(CO6)(Understand/LOCQ)]*

8 + 4 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	33.33	54.17	12.5

Course Outcome (CO):

After the completion of the course students will be able to

CSBS2202.1. Categorize the types of instructions and addressing modes and their impact on processor design.
CSBS2202.2. Demonstrate the design of the arithmetic and logical units of a digital computer system.
CSBS2202.3. Analyze performance and techniques to improve the performance of cache memory organization to reduce the access time.
CSBS2202.4. Illustrate the concepts of paging, segmentation, segmentation with paging, and page replacement strategies in the paradigm of virtual memory to create the illusion of a large memory of a computer system.
CSBS2202.5. Explain the pipeline techniques for consistent execution of instructions with minimum hazards.
CSBS2202.6. Understand the concepts of parallel processing, multiprocessor architectures and control unit design.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*