B.TECH/AEIE/5TH SEM/AEIE 3102/2016

MICROPROCESSOR — ARCHITECTURE & APPLICATIONS
(AEIE 3102)

Time Allotted : 3 hrs **Full Marks : 70**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 5 (five) from Group B to E, taking at least one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A
(Multiple Choice Type Questions)

1. Choose the correct alternative for the following: **10 × 1 = 10**

(i) Address bus of 8085 µP is -
(a) 8 bit unidirectional (b) 8 bit bidirectional
(c) 16 bit bidirectional (d) 16 bit unidirectional.

(ii) The control signal used to distinguish between an I/O operation and memory operation is -
(a) ALE (b) IO/ $\overline{M}$ (c) SID (d) READY.

(iii) LDA 2050H is a ____ instruction
(a) 1 byte (b) 2 byte (c) 3 byte (d) 4 byte.

(iv) The no of T-States required for MOV B,M is -
(a) 4 (b) 7 (c) 10 (d) None of these.

(v) Whenever the POP H instruction is executed-
(a) data bytes in HL register pair are stored on the stack
(b) two data bytes from stack are transferred to HL register pair
(c) two data bytes from stack are transferred to PC
(d) none of these.

(vi) For 8255 PPI the bi-directional mode of operation is supported in -
(a) Mode 0 (b) Mode 1
(c) Mode 2 (d) BSR Mode.

(vii) Mode 2 of 8253 is -
(a) square wave generator (b) rate generator
(c) software trigger strobe (d) hardware trigger strobe.

(viii) PSW is a ___ register
(a) 8 bit (b) 16 bit (c) 32 bit (d) 12 bit.

(ix) If CWR address of 8255 connected to 8085 is FB_H, then address for Port A is -
(a) $F8_H$ (b) FA_H (c) FC_H (d) $F9_H$.

(x) The call location for TRAP interrupt is -
(a) 0000_H (b) 0020_H
(c) 0024_H (d) 0034_H.

Group – B

2. (a) Describe the process of demultiplexing of multiplexed address-data bus (AD0-AD7) in 8085A with suitable circuit diagram.

(b) Discuss the function of following signals (*Any four*) –
(i) ALE (ii) $\overline{INTA}$ (iii) READY (iv) HOLD (v) X1-X2.

(c) Explain the function of following instructions (*Any three*) –
(i) LDAX B (ii) SHLD E000H (iii) CMA (iv) DAA.

5 + 4 + 3 = 12

3. (a) Discuss the different addressing modes of 8085 µP with suitable example.

(b) Discuss the difference between SUB and CMP instructions.

(c) Write a program to find the 2's complement of a 8 bit number stored at memory location 8100_H.

5 + 3 + 4 = 12

Group – C

4. (a) Define – Instruction cycle, Machine cycle and T state.

(b) With the help of timing diagram explain the sequence of events that occur for the execution of ADI $4F_H$ instruction. Assume that the opcode of the instruction is XX_H and it is stored in memory location 8000_H. Also calculate the time required to execute the instruction where the clock frequency is 3 MHz

(c) What do you mean by Non-Maskable (NMI) and Vectored Interrupt?

3 + 7 + 2 = 12

5. (a) With suitable example explain PUSH and POP instructions.

(b) Draw and discuss SIM instruction format.

(c) Write a program to enable the interrupts in 8085 μP and to mask RST 5.5, RST 7.5 and unmask RST 6.5 interrupts.

(d) Using a single 8 bit register write a delay subroutine.

3 + 4 + 3 + 2 = 12

Group – D

6. (a) What is the difference between absolute and partial address decoding?

(b) Design an interface between 8085 μP and one 8KB RAM memory chip using 3:8 decoder to generate the chip select signal. Select suitable memory map.

(c) Why multiplexed bus is used in 8085 μP?

2 + 8 + 2 = 12

7. (a) Interface an 8 bit DIP switch and 8 LEDs with 8085 μP, such that the address assigned to them are FE_H and FA_H, respectively. Write a program to read the status of the switches and display the status to the LEDs repeatedly.

(b) What are the differences between memory mapped I/O and I/O mapped I/O schemes?

8 + 4 = 12

Group – E

8. (a) Draw and discus the control word register (CWR) format of 8255 PPI in I/O mode.

(b) What do you mean by Mode 0, Mode 1 and Mode 2 operation of 8255 PPI?

(c) Write an assembly language program for 8085 μP to periodically turn ON and OFF two switches by setting 8255 PPI to BSR mode. The duty cycle is 50%.

3 + 4 + 5 = 12

9. (a) What is the purpose of Priority Resolver in 8259A? How they will resolve priority? Describe with a suitable diagram.

(b) List the various operating modes of 8254.

(c) Write a program to set up 8254 as a square wave generator with a period of 1 sec. Assume that the input frequency to 8254 is 1 MHz.

5 + 2 + 5 = 12