COMPUTER ORGANIZATION AND ARCHITECTURE
(CSEN 2202)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Conflict miss is zero, in case of
(a) direct cache mapping (b) fully associative cache mapping
(c) set-associative cache mapping (d) all of these.

(ii) In an accumulator based machine, an instruction explicitly specifies how many operands?
(a) 0 (b) 1 (c) 2 (d) More than 2.

(iii) An external controller directly transfers data between memory and I/O devices without CPU intervention. What kind of data transfer mechanism is this?
(a) Programmed I/O (b) Interrupt driven I/O
(c) Memory mapped I/O (d) DMA.

(iv) The time required to complete 15 tasks in a 6-stage pipelined processor with 1 MHz clock cycle is
(a) 90 μsec (b) 50 μsec (c) 20 μsec (d) 5 μsec.

(v) In a SIMD machine consisting of 'n' PEs arranged in a 1-D array,
(a) odd even transposition sorting runs in O(n) time on n elements
(b) two n x n matrices can be added in O(n) time
(c) two n x n matrices can be multiplied in $O(n^2)$ time
(d) all of these.

(vi) In the segmentation technique of Virtual Memory, the segment table contains base address as 1000 and offset as 300 for page # 1. What is the physical address corresponding to the logical address (1, 150)?
(a) 450 (b) 1150 (c) 1300 (d) gives rise to ERROR

(vii) An initial collision vector is "1011010" for a pipeline. The corresponding reservation table has three rows with 3, 2 and 3 cross marks respectively. The lower and upper bounds of MAL for this pipeline are:
(a) 2,2 (b) 2,3 (c) 3,3 (d) 3,4.

(viii) Cycle stealing happens in case of
(a) Programmed IO (b) Non Maskable Interrupt
(c) Maskable Interrupt (d) Direct Memory Access.

(ix) Which of the following statements is correct?
(a) Vector processors can have CPI less than 1
(b) Vector chaining is analogous to pipelining
(c) Without horizontal interleaving, vector memory access units can perform one memory operation per cycle
(d) Vector processing does not allow multiple functional pipelined units.

(x) A 64 input Omega Network requires how many stages of 2 × 2 switches?
(a) 4 (b) 6 (c) 8 (d) 64.

Fill in the blanks with the correct word

(xi) The value of shuffle(exchange(10110101_2) is _____.

(xii) A RISC machine has _____ instruction format.

(xiii) In a Direct Mapping Cache, there are 16 cache lines and 128 memory blocks. The memory block # 37 will be mapped into cache line Number _____.

(xiv) An instruction fetched from memory is brought to _____ register.

(xv) The total number of crossbar modules required in a 4^3 X 4^3 delta network is ____.

Group - B

2. (a) What are the addressing modes for the following instructions?
(i) MOV R_1, *R_2+ (ii) ADD (iii) BR $ -5. *[(CO1)(Apply/IOCQ)]*

(b) A 25 MHz processor is used to execute a program with the following instruction mix:

Instruction Type	Instruction Count	Clock Cycles required per instruction
Data Transfer	6000	3
Integer Arithmetic	4600	2
Floating Point Arithmetic	3000	1
Branch	400	4

Calculate the effective CPI, MIPS and execution time for this program. *[(CO1)(Evaluate/HOCQ)]*

(c) Consider the instruction "Load A, R1", which means value is read from memory location A into the CPU register R1. Describe the sequence of steps needed for the CPU to fetch and execute the above instruction. You may assume any suitable CPU architecture. *[(CO2)(Understand/IOCQ)]*

(d) In general, memory access time is 100 times more than a single CPU operation time. But in a RISC machine, use of a fast L1 cache ensures that memory access stage takes about the same time (i.e. one cycle) as other stages working within the CPU. Mention two techniques, with proper justification, through which a RISC machine uses the L1 cache to achieve this goal. *[(CO2)(Analyze/HOCQ)]*

3 + 3 + 3 + 3 = 12

3. (a) In a computer, there are 30 processor Registers, 6 addressing modes and 32k x 32 main memory. Each instruction (having size of 32 bits) supports one register operand and one memory address operand. State the instruction format, after finding out the size of each field. *[(CO1)(Evaluate/IOCQ)]*

(b) Specify the different types of control signals generated in each stage for the execution of the instruction Move (R1),R2. *[(CO4)(Remember/IOCQ)]*

(c) Hardwired control unit is used in a CPU, the instruction format of which is given below:

OPCODE (4 bits)	MODE (3 bits)	Address (9 bits)

(i) What type of decoder will be required for instruction decoding?
(ii) To generate 32 timing signals, what type of counter and decoder will be required? *[(CO1)(Analyse/IOCQ)]*

4 + 4 + 4 = 12

Group - C

4. (a) How are "Tag" bits used in cache memory systems? Explain with reference to the three cache mapping techniques. *[(CO3)(Analyze/IOCQ)]*

(b) Consider the following sequence of memory references:
1,2,1,3,7,4,5,6,3,1
The cache memory can hold three blocks and is initially empty. How many misses occur for the following replacement policies?
(i) LRU (ii) FIFO. *[(CO3)(Understand/LOCQ)]*

(c) In a 4-way set-associative cache mapping, the cache size is 64KWords and the size of the main memory is 16 MWords. The main memory is divided into a number of blocks, each of size 2 KWords. Find the number of bits for tag, set and word offset. Find out the set number in Hex if the block number is $0BAD_{16}$. *[(CO3)(Apply/IOCQ)]*

3 + (3 + 2) + 4 = 12

5. (a) State one advantage and one disadvantage of memory-mapped IO, compared to IO-mapped IO. *[(CO4)(Understand/LOCQ)]*

(b) What is NMI? Give examples. *[(CO4)(Remember/LOCQ)]*

(c) Describe step-by-step what happens when the CPU is interrupted while it was executing the i^{th} instruction of a program. *[(CO4)(Apply/IOCQ)]*

(d) Describe briefly, the sequence of events involved in DMA Transfer. *[(CO4)(Understand/IOCQ)]*

2 + 2 + 3 + 5 = 12

Group - D

6.

	1	2	3	4	5	6	7
S1	X						X
S2		X		X			
S3			X		X		

For the reservation table above, please answer the following questions.
(i) Determine Forbidden Latency, Permissible Latency and Initial Collision Vector.
(ii) Draw the permissible state diagram. List all simple cycles, especially pointing out the Greedy Cycles (GC).
(iii) What is Minimum Average Latency (MAL) of the pipeline? Is there any GC corresponding to this MAL?
(iv) What is the lower bound on this MAL (i.e. Minimum Achievable Latency)? What is the upper bound?

[(CO2)(Understand/IOCQ)]

[3 + (3 + 2) + (1 + 1) + (1 + 1)] = 12

7. (a) How can hazard occur in executing the following set of instructions?

I1: MOV R1,A
I2: ADD R2,R3
I3: SUB R4,R5
I4: NOP

All the symbols have their usual meanings.
You may assume a pipeline unit consisting of four stages. *[(CO2)(Analyze/IOCQ)]*

(b) Consider the following program being executed on a vector processor.

For I=0 to 49
C(I) = A(I) + B(I)

Show the sequence of vector instructions for the above program. Also calculate how many cycles will be needed by the vector processor to complete the same. *[(CO2/CO6)(Apply/IOCQ)]*

(c) How can use of vector chaining improve performance if we add the following line to the program in (b)?

E(I) = C(I) + D(I). *[(CO2/CO6)(Apply/HOCQ)]*

4 + (3 + 2) + 3 = 12

Group - E

8. (a) Show in detail how the following two matrices are multiplied on an SIMD machine where PEs are stored in a 2D Mesh:

$$\begin{pmatrix} 1 & 2 & 1 \\ 2 & 1 & 2 \\ 1 & 2 & 2 \end{pmatrix} \text{ X } \begin{pmatrix} 2 & 2 & 1 \\ 2 & 3 & 3 \\ 1 & 1 & 1 \end{pmatrix}$$

Comment on the computation and routing complexity. *[(CO6)(Apply/LOCQ)]*

(b) As we run the matrix multiplication algorithm on SIMD machines with more and more number of processing elements N, the computation complexity keeps on getting reduced. Justify this with the 1-D array, the 2-D Mesh and the Hypercube architecture. What happens to the routing complexity in each of the above cases? *[(CO6)(Understand/IOCQ)]*

(c) In what way a single stage cube network differs from a multi stage implementation of the same? *[(CO6)(Analyze/IOCQ)]*

(4 + 2) + 3 + 3 = 12

9. (a) Describe the perfect shuffle - exchange operation with an example. *[(CO5)(Remember/LOCQ)]*

(b) Draw the diagram of a multi-stage 8 X 8 Omega network. On the diagram show the path (alongwith switch settings) for routing a message from node 001 to node 100 and from node 011 to node101 simultaneously. State with reasons whether blocking exists in this case. *[(CO5)(Analyse/IOCQ)]*

(c) Consider a modified hypercube network. Here instead of each node, four nodes are placed connected in a cycle. Suggest a suitable node addressing scheme in this network. Also show the possible routing functions. *[(CO5)(Apply/HOCQ)]*

2 + (4 + 1 + 1) + (2 + 2) = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	17.71	68.75	13.54

Course Outcome (CO):

After the completion of the course students will be able to
CO1. Understand the basic organization of computer and different instruction formats and addressing modes.
CO2. Analyze the concept of pipelining, segment registers and pin diagram of CPU.
CO3. Understand and analyze various issues related to memory hierarchy.
CO4. Understand various modes of data transfer between CPU and I/O devices.
CO5. Examine various inter connection structures of multi-processor.
CO6. Design architecture with all the required properties to solve state-of-the-art problems.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*