# DIGITAL ELECTRONICS
## (AEIE 2201)

**Time Allotted: 2½ hrs** **Full Marks : 60**

***Figures out of the right margin indicate full marks.***

***Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.***

***Candidates are required to give answer in their own words as far as practicable.***

1. Answer any twelve: **12 × 1 = 12**

*Choose the correct alternative for the following*

(i) The given hexadecimal number $(1E.53)_{16}$ is equivalent to
(a) $(35.684)_8$ (b) $(36.246)_8$
(c) $(34.340)_8$ (d) $(35.599)_8$

(ii) 2 input XOR gate behave as a NOT gate when
(a) both inputs are at logic 1 (b) both inputs are at logic 0
(c) one input is at logic 1 (d) one input is at logic 0

(iii) On subtracting $(010110)_2$ from $(1011001)_2$ using 2's complement, we get
(a) 0111001 (b) 1100101
(c) 0110110 (d) 1000011

(iv) A full adder logic circuit will have
(a) two inputs and one output (b) three inputs and three outputs
(c) two inputs and two outputs (d) three inputs and two outputs.

(v) For addition, Carry look ahead logic uses the concepts of
(a) Inverting the inputs (b) Complementing the outputs
(c) Generating and propagating carries (d) Ripple factor.

(vi) How is a J-K flip-flop made to toggle?
(a) J = 0, K = 0 (b) J = 1, K = 0
(c) J = 0, K = 1 (d) J = 1, K = 1.

(vii) Which of the following flip-flop is free from the race around the problem?
(a) T flip-flop (b) SR flip-flop
(c) Master-Slave Flip-flop (d) D flip-flop.

(viii) The term synchronous means
(a) the output changes state only when any of the input is triggered
(b) the output changes state only when the clock input is triggered
(c) the output changes state only when the input is reversed
(d) the output changes state only when the input follows it.

(ix) Transistor–transistor logic (TTL) is a class of digital circuits built from
(a) JFET only
(b) Bipolar junction transistors (BJT)
(c) Resistors
(d) Bipolar junction transistors (BJT) and resistors.

(x) The difference between a PAL & a PLA is
(a) PALs and PLAs are the same thing
(b) The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
(c) The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
(d) The PAL has more possible product terms than the PLA.

*Fill in the blanks with the correct word*

(xi) A product term containing all K variables of the function in either complemented or uncomplemented form is called a _____ .

(xii) The output of a binary to gray code converter is ____ for the input 100101.

(xiii) A decimal counter has _____ states.

(xiv) Realization of 8:1 Multiplexer requires _____ number of 2:1 Multiplexer/s.

(xv) _____ flip-flops are required to construct a decade counter.

## Group - B

2. (a) Realize (i) an EX-OR gate using NOR gate, (ii) an Inverter using only EX-OR gate. *[(CO2)(Apply/IOCQ)]*

(b) Convert $(A7F.E2)_{16} = (??)_8$ *[(CO1)(Apply/IOCQ)]*

(c) Design and analyze full adder circuit using 8:1 multiplexer. *[(CO3)(Create/HOCQ)]*

**(3 + 2) + 2 + 5 = 12**

3. (a) Convert $(1100101.101101)_2 = (??)_8$. *[(CO1)(Apply/IOCQ)]*

(b) Find the value of P if $(237)_4 = (702)_P$. *[(CO1)(Apply/IOCQ)]*

(c) Implement the logic function $Y(A,B,C,D) = \sum m(0,2,5,7,9,11,12,14)$ by using 4:1 multiplexer. *[(CO3)(Apply/IOCQ)]*

**2 + 3 + 7 = 12**

## Group - C

4. (a) Minimize the logic function $Y(A,B,C,D) = \sum m(1,3,4,6,8,10,13,15) + \sum d(5,7)$ by using Karnaugh map. *[(CO3)(Apply/IOCQ)]*

(b) Minimize the logic function $Y = \sum m(1,3,4,8,9,11,12,17,19,20,24,25,27,28)$. *[(CO3)(Apply/IOCQ)]*

**6 + 6 = 12**

5. (a) What is the difference between combinational and sequential circuit? *[(CO4)(Remember/LOCQ)]*

(b) Design and analyze an S-R flip flop using logic gates with truth table. *[(CO4)(Understand/LOCQ)]*

(c) Design a D- flip flop using S-R flip flop with truth table. *[(CO4)(Understand/LOCQ)]*

**3 + (3 + 2) + 4 = 12**

## Group - D

6. (a) Design and analyze the operation of a decade counter. *[(CO3)(Apply/IOCQ)]*

(b) Design and analyze an asynchronous counter having 16 different output states. *[(CO4)(Apply/IOCQ)]*

**6 + 6 = 12**

7. (a) Design a ripple counter to start the count at 4 and stop the count at 6 and start the count again from 4. *[(CO4)(Create/HOCQ)]*

(b) Design a MODULO-8 synchronous counter and explain with output waveforms. *[(CO4)(Apply/IOCQ)]*

**6 + 6 = 12**

## Group - E

8. (a) Compare Implement the given functions using programmable logic array (PLA) $X(a,b,c)=\sum m(0,2,4,5)$, $Y(a,b,c)=\sum m(1,3,6,7)$. *[(CO5)(Apply/IOCQ)]*

(b) Compare between logic Families: TTL, ECL, and CMOS. *[(CO6)(Remember/LOCQ)]*

**6 + 6 = 12**

9. (a) Write short notes on Dual slope type ADC and Binary weighted DAC. *[(CO5)(Understand/LOCQ)]*

(b) Design a NOR gate using CMOS logic. *[(CO6)(Understand/LOCQ)]*

**(4 + 6) + 2 = 12**

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| Cognition Level | LOCQ | IOCQ | HOCQ |
|---|---|---|---|
| Percentage distribution | 31.25 | 57.29 | 11.46 |

**Course Outcome (CO):**

After the completion of the course students will be able to

1. Understand the fundamentals of converting from one number system to another.
2. Explain the basic logic operations of NOT, AND, OR, NAND, NOR, and XOR.
3. Analyze, design and implement combinational logic circuits.
4. Analyze, design and implement sequential logic circuits.
5. Describe the nomenclature and technology in the area of memory devices: ROM, PROM, PLD etc. and different kind of ADCs and DACs.
6. Understand the basic operating principles of different logic families.

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*