VLSI IC FABRICATION
(VLSI 5132)

Time Allotted : 2½ hrs **Full Marks : 60**

Figures out of the right margin indicate full marks.

Candidates are required to answer Group A and any 4 (four) from Group B to E, taking one from each group.

Candidates are required to give answer in their own words as far as practicable.

Group – A

1. Answer any twelve: **12 × 1 = 12**

Choose the correct alternative for the following

(i) Optical Masking is used for
(a) pattern transfer (b) oxidation
(c) protection (d) cleaning.

(ii) p-well is created on
(a) p-substrate (b) n-substrate
(c) p and n substrate (d) insulator.

(iii) Oxidation is used for
(a) isolation (b) interconnection
(c) doping (d) packaging.

(iv) Epitaxial Growth of Silicon on Sapphire (SoS) means
(a) Homoepitaxi (b) Heteroepitaxi
(c) Vertical Epitaxi (d) None of these.

(v) The damage in the ion-implanted sample is primarily due to
(a) Electronic stopping
(b) Nuclear stopping
(c) A combination of electronic and nuclear stopping
(d) None of the above.

(vi) Assuming constant diffusivity, the doping profile for an infinite source diffusion process can be approximated as
(a) Gaussian (b) Exponential
(c) Erfc (d) None of these

(vii) A clean room is controlled environment, where
(a) products are manufactured (b) products are stored
(c) products are displayed (d) none of these.

(viii) In semiconductor manufacturing, "lithography" is used
(a) to dope semiconductors
(b) to deposit amorphous films on semiconductors
(c) to deposit polycrystalline films on semiconductors
(d) to produce patterns in the films deposited on semiconductors.

(ix) Ion implantation is a technique to
(a) dope a semiconductor
(b) deposit an insulating layer on a semiconductor
(c) deposit a metallic layer on a semiconductor
(d) deposit a metallic layer on an insulator.

(x) For Industrial epitaxial growth reactors are
(a) Vertical type (b) Barrel type
(c) Horizontal type (d) None of these.

Fill in the blanks with the correct word

(xi) Sputtering is a ____________ process.

(xii) The damage in the ion-implanted sample is primarily due to _______ stopping.

(xiii) Photoresist is a ____________compound.

(xiv) Heavily doped polysilicon is deposited using ____________.

(xv) Both gate and field oxides, are generally grown by the process of ________.

Group - B

2. (a) Describe the requirements and conditions for the VLSI fabrication lab. *[(CO1)(Understand/LOCQ)]*
(b) Explain the necessity of special clean room garments for working in VLSI Lab. *[(CO1)(Understand/LOCQ)]*
(c) Illustrate the reasons that the 'Photolithography is preferred to be done in a"Class-10" clean room' and in 'yellow light'? *[(CO3)(Analyse/IOCQ)]*

4 + (2+2) + 4 = 12

3. (a) Mention the uses of SiO_2 in the IC fabrication industry. *[(CO2)(Remember/LOCQ)]*
(b) Differentiate between dry and wet oxidation. Write down the corresponding chemical equations. *[(CO2)(Understand/LOCQ)]*
(c) Explain with a suitable schematic diagram a typical horizontal tube oxidation furnace set-up. *[(CO2)(Understand/LOCQ)]*

4 + 3 + 5 = 12

Group - C

4. (a) Discuss the advantages of doping using ion implantation method over the diffusion method. *[(CO4)(Analyze/IOCQ)]*

(b) Explain the basic principle of operation of an ion-implantation system with a suitable diagram. *[(CO4)(Understand/LOCQ)]*

5 +7 = 12

5. (a) Describe with an appropriate diagram, an electron-beam lithography system. *[(CO3) (Remember/LOCQ)]*

(b) Explain the advantages of thermal oxidation. *[(CO5)(Analyse/IOCQ)]*

(c) Use the LSS theory to calculate the implant dose required to give a peak dopant concentration of $5x10^{18}$ boron atoms cm^{-3} in an n-type Si, doped with 10^{15} phosphorous atoms $cm^{-3}$when boron is implanted at 200 keV into Si. Given the lateral straggle for boron ions at 200 keV is 0.086 micron. *[(CO3)(Evaluate/HOCQ)]*

4 + 3 + 5 = 12

Group - D

6. (a) What is wet chemical etching? *[(CO3)(Remember/LOCQ)]*

(b) What are the characteristics of an ideal etchant used for wet chemical etching? *[(CO3)(Remember/LOCQ)]*

(c) In Optical lithography, which parameter fundamentally determines the minimum resolvable feature size? Explain your answer briefly. *[(CO3)(Analyze/IOCQ)]*

2 + 4 + 6 = 12

7. (a) State the principal limitations of conventional lithography. How are these overcome in electron-beam lithography? *[(CO4)(Apply/IOCQ)]*

(b) What is a positive photoresist? Explain with suitable diagrams the steps of pattern transfer using a negative photoresist. *[(CO4)(Remember/LOCQ)]*

(3 + 3) + (2 + 4) = 12

Group - E

8. (a) What is epitaxy? *[(CO5)(Remember/LOCQ)]*

(b) Why is epitaxial growth necessary during device fabrication? *[(CO5)(Understand/LOCQ)]*

(c) Discuss the sputtering technique of film deposition. *[(CO5)(Analyze/HOCQ)]*

3 + 3 + 6 = 12

9. (a) What is self aligned gate? How is it formed, and what is the necessity of it? *[(CO6)(Analyse/IOCQ)]*

(b) Compare between the MOSFET and MESFET fabrication technologies. *[(CO6)(Remember/LOCQ)]*

(2 + 4) + 6 = 12

Cognition Level	LOCQ	IOCQ	HOCQ
Percentage distribution	57.29	31.25	11.45

Course Outcome (CO):

After the completion of the course students will be able to

1. Students will learn clean room concepts
2. Students will learn individual fabrication steps
3. Students will learn Pattern Transfer to Si from Mask using Lithography
4. Student will learn semiconductor doping techniques
5. Student will learn planner MOSFET fabrication process
6. Student will learn SOI fabrication Technology

**LOCQ: Lower Order Cognitive Question; IOCQ: Intermediate Order Cognitive Question; HOCQ: Higher Order Cognitive Question.*